

Project Namel: Gambit MLK MT
PCB Number: 17529
PCBA Ver.: A00
SCH Ver.: A00
Project Code : 3PD0A2010001
PCB Size: 257.4 x 244mm, 1.6mm, 4 Layers

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| 65 | (R) |
| 66 | (R) |
| 67 | (R) |
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| 69 | (R) |
| 70 | (R) |
| 71 | (R) |
| 72 | (R) |
| 73 | (R) |
| 74 | (R) |
| 75 | (R) |
| 76 | (R) |
| 77 | (R) |
| 78 | (R) |
| 79 | (R) |
| 80 | (R) |
| 81 | (R) |
| 82 | (R) |
| 83 | (R) |
| 84 | (R) |
| 85 | (R) |
| 86 | (R) |
| 87 | (R) |
| 88 | (R) |
| 89 | (R) |
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| 107 | Change Histroy |

Jumper Setting

| JMP1 | Pin 1-2 | With Jumper to ME Disable |
|------|---------|--------------------------------------|
| | Pin 3-4 | Without Jumper to Clear Password |
| | Pin 5-6 | With Jumper to Clear CMOS |
| DB1 | PD 1K | PD 1K to GND for Debug, All Power-On |

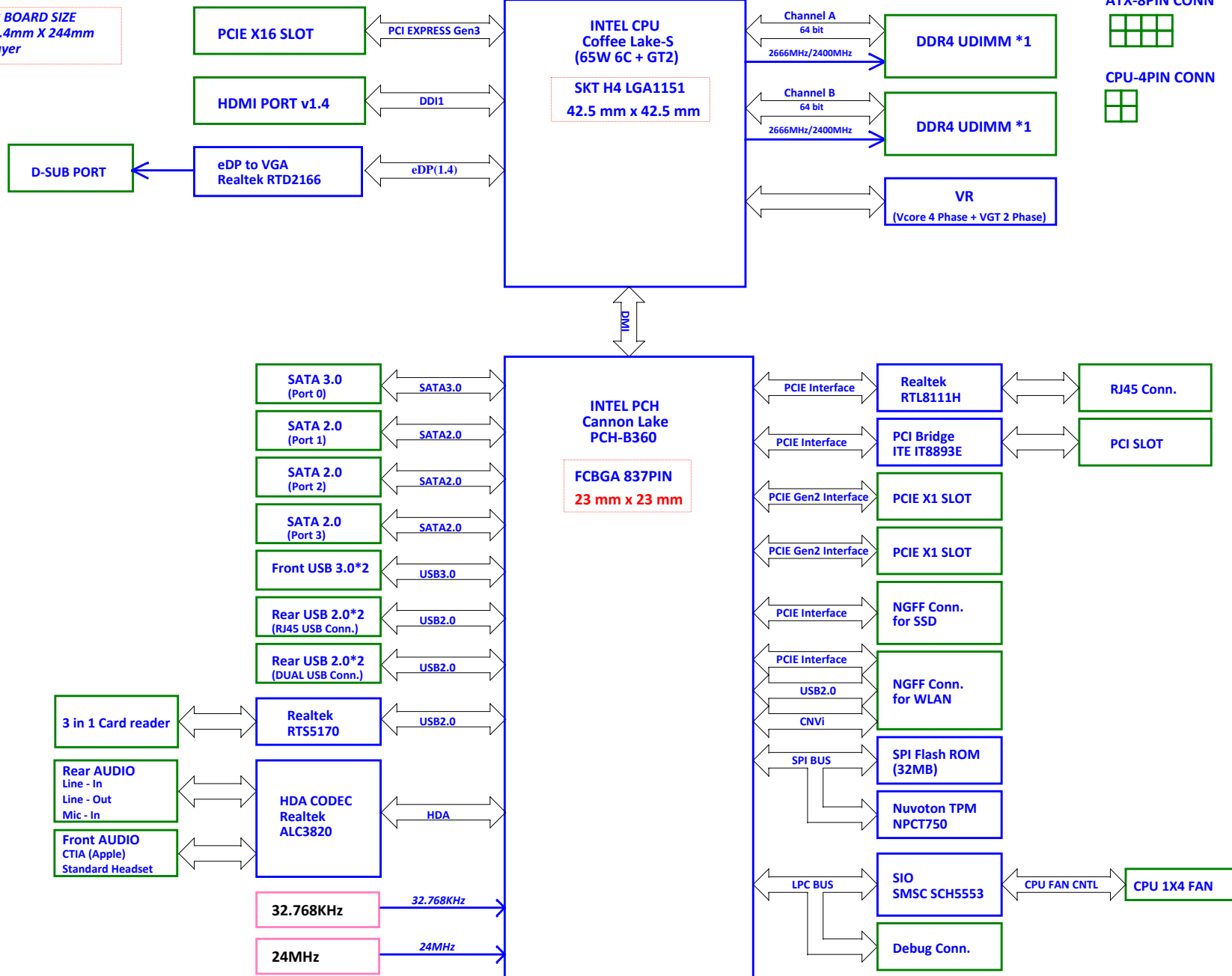
BOM Configuration

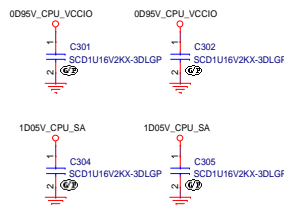
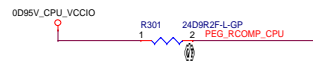
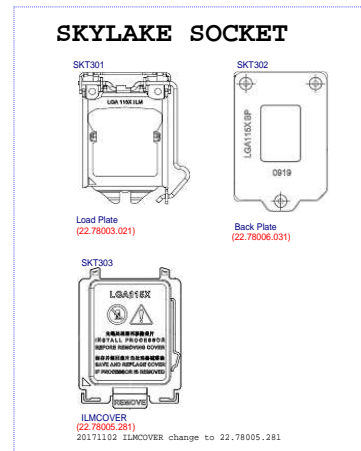
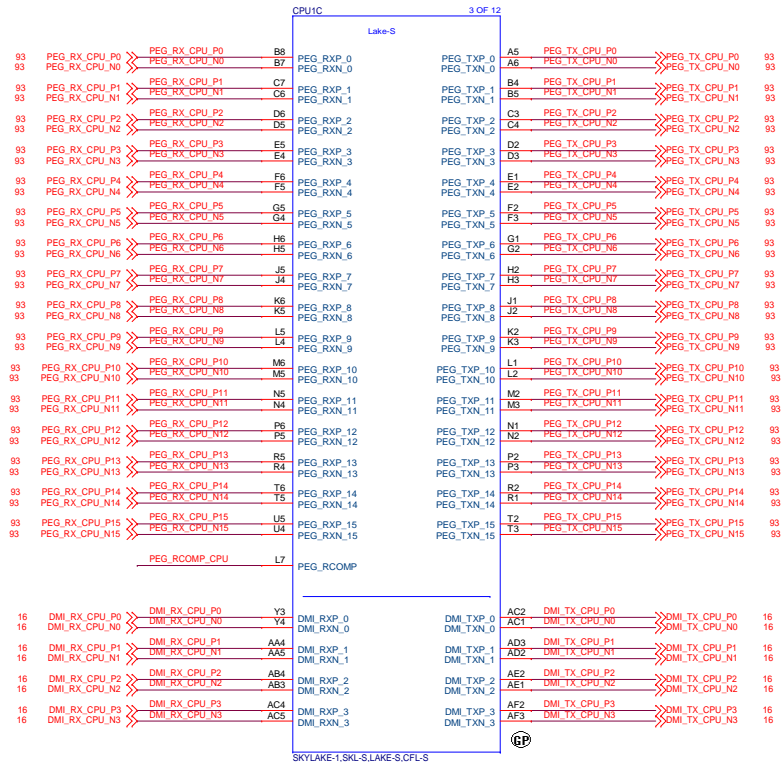
(R_): Unmount
(X_): Debug
(GAM_): Gambit MLK MT
(EAG_): Eagle MT
(TPM_): TPM function
(NONTPM_): non-TPM function

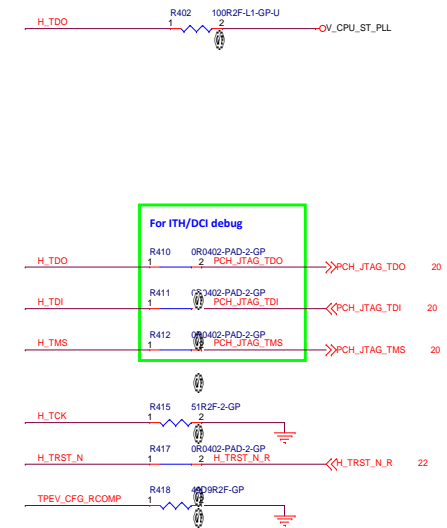
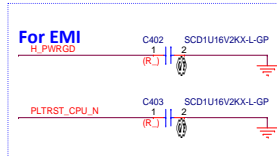
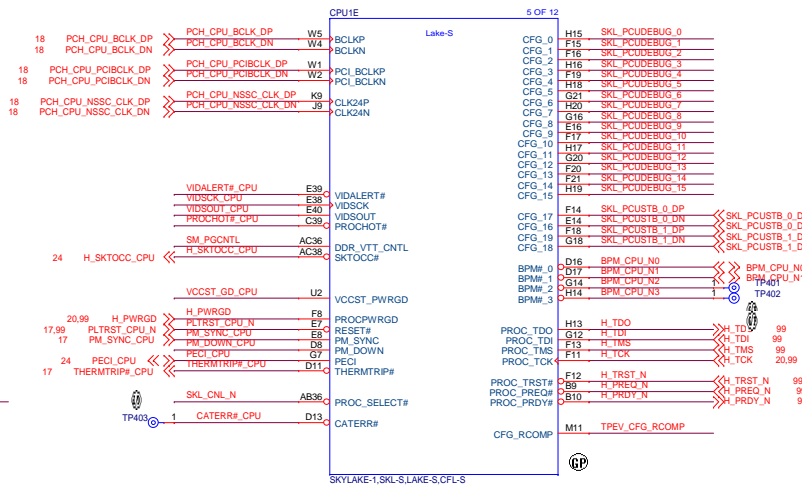
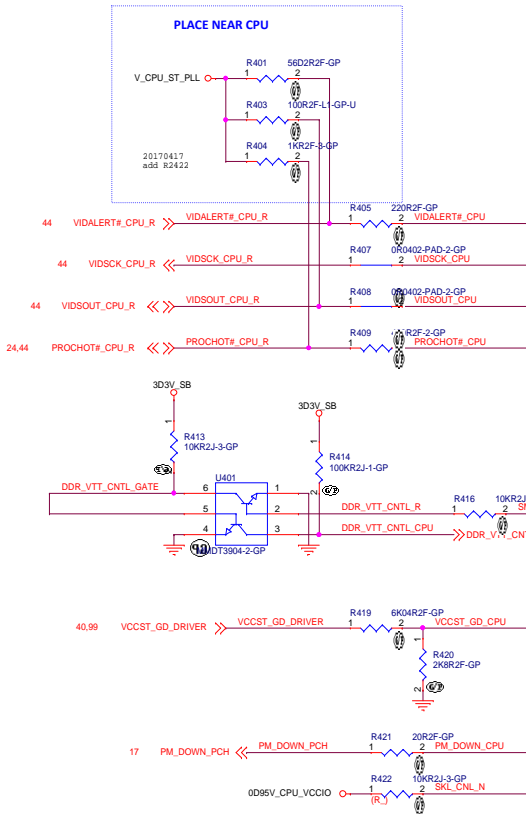
Power sates

| | Name | G3 | DSW | S5 | S4 | S3 | S0 |
|------|--------------------|----|-----|----|----|----|----|
| +12V | V_12P0_A | | O | O | O | O | O |
| | +12V | | | | | | O |
| | V_12V_CPU_S0 | | O | O | O | O | O |
| -12V | -12V | | | | | | O |
| | 5V_S0 | | | | | | O |
| +5V | USBVCC12 | | | | | | |
| | USBVCC34 | | | O | O | O | O |
| | USBVCC78 | | | | | | |
| | 5V_S5 | | | | | | |
| | V_5_CODEC | | O | O | O | O | O |
| | 3P3V_S0 | | | | | | O |
| | 3P3V_AUD_S0 | | | | | | |
| 3.3V | 3P3V_SB | | | | | | |
| | 3P3V_SPI | | | O | O | O | O |
| | 3P3V_LAN | | | | | | |
| | 3P3V_M2VAUX | | | | | | |
| | 3P3V_PCIVAUX | | | | | | |
| | 3P3V_S5 | | O | O | O | O | O |
| VBAT | 3P0V_BAT_VREG | | | | | | |
| | VBAT1 | O | O | O | O | O | O |
| | VBAT2 | | | | | | |
| VDDQ | +VCCPLL_OC | | | | | | O |
| | V_SM | | | | | O | O |
| DIMM | V_SM_VTT | | | | | | O |
| | V_VPP | | | | | | |
| PCH | V1P0_PCH_SB | | | | | | |
| | +V1P0A_VCCAPLL | | | | | | |
| | +V1P0A_VCCF24_1P0 | | | | | | |
| | +V1P0A_VCCAMPHYPLL | | | O | O | O | O |
| | V_CPU_ST_PLL | | | | | | |
| CPU | V_CPU_CORE | | | | | | |
| | V_CPU_GT | | | | | | |
| | V_CPU_IO | | | | | | O |
| | V_CPU_SA | | | | | | |
| | +VCCFUSEPRG | | | | | | |

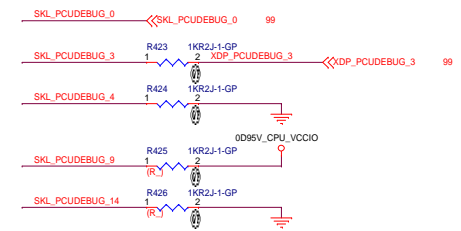
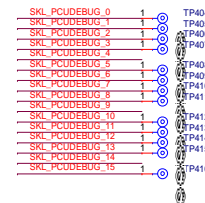
PCB BOARD SIZE
257.4mm X 244mm
4 Layer

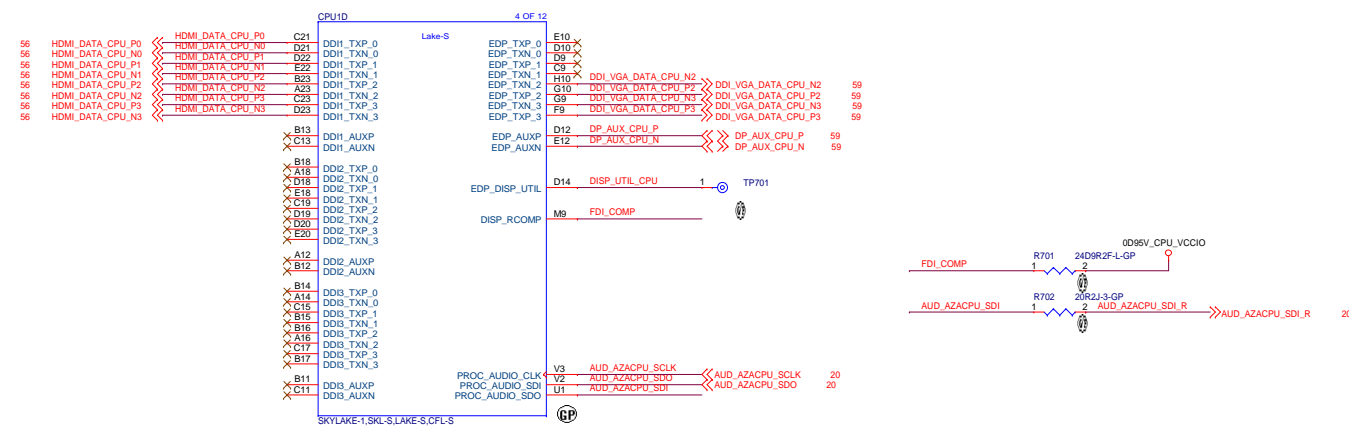


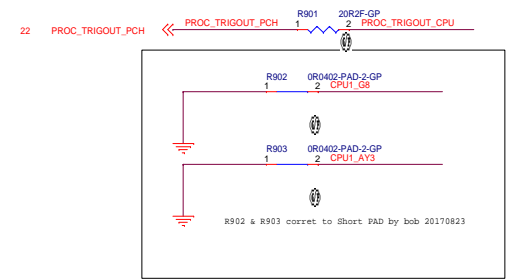
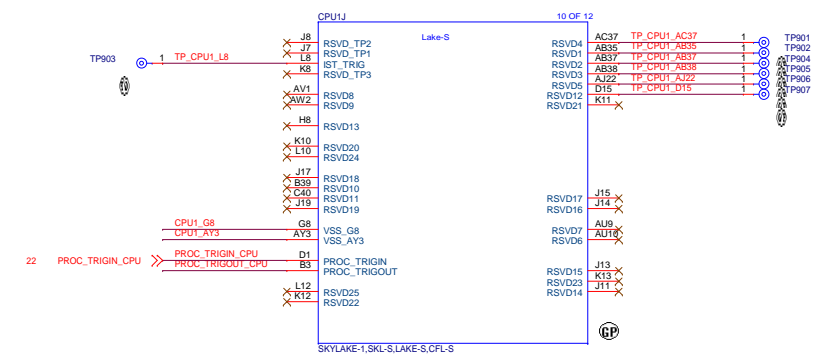
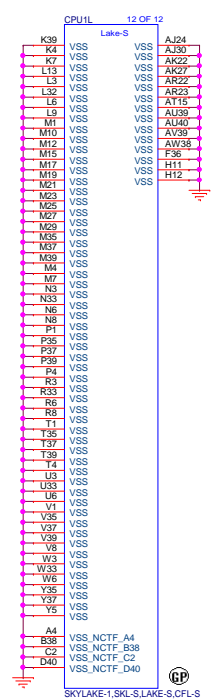
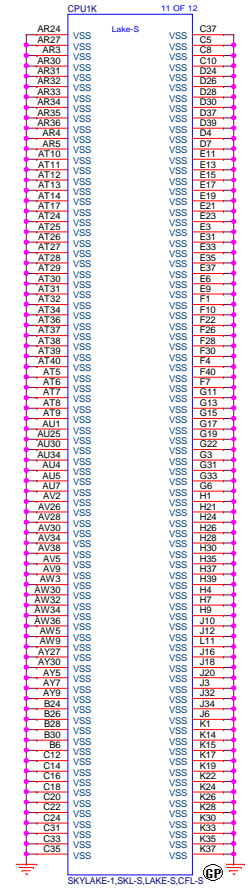
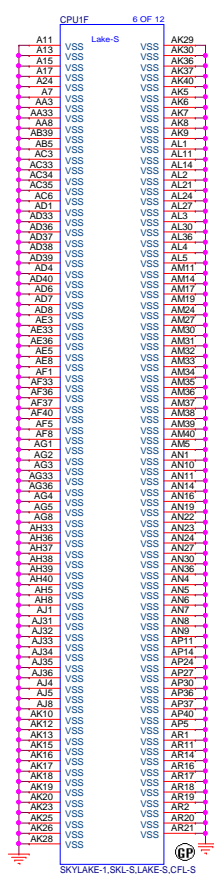


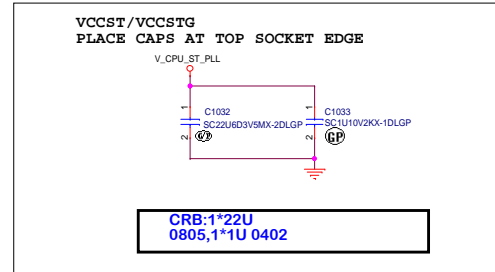
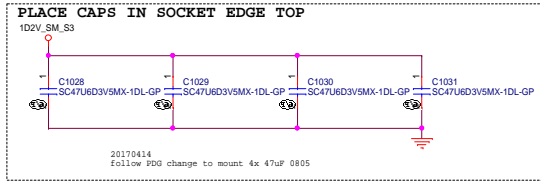
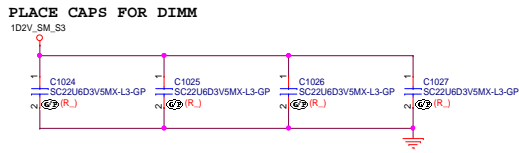
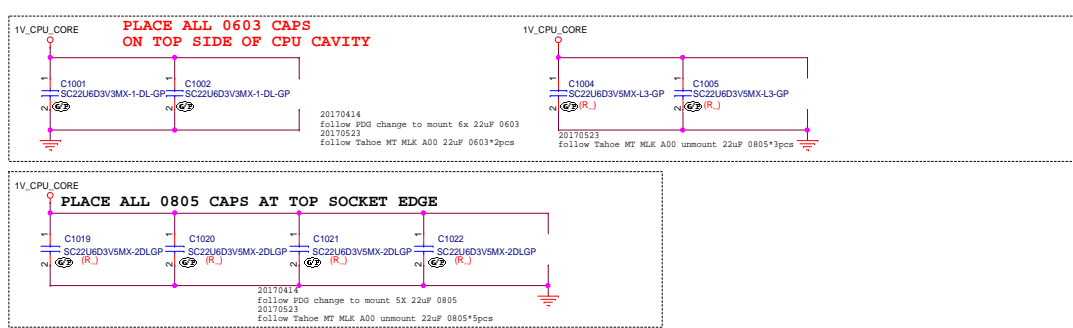
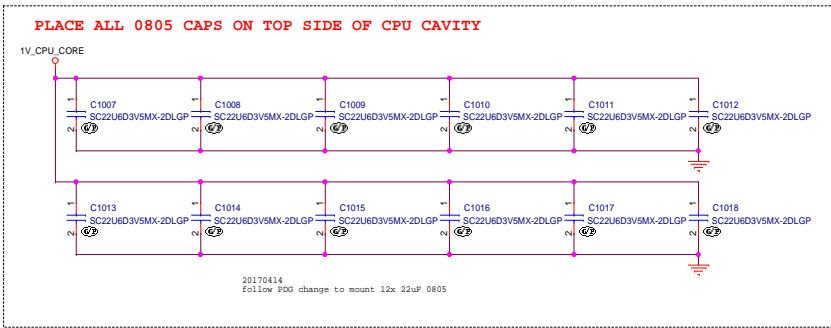


| Signal Name | Description | Dir. | Buffer Type | Link Type | Availability |
|-------------|---|------|-------------|-----------|---|
| CFG[19:0] | <p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: <ul style="list-style-type: none"> 1 = (Default) Normal Operation; No stall. 0 = Stall. CFG[1]: Reserved configuration lane. CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> 1 = Normal operation 0 = Lane numbers reversed. CFG[3]: Reserved configuration lane. CFG[4]: eDP enable: <ul style="list-style-type: none"> 1 = Disabled. 0 = Enabled. CFG[6:5]: PCI Express* Bifurcation <ul style="list-style-type: none"> 00 = 1 x8, 2 x4 PCI Express* 01 = reserved 10 = 2 x8 PCI Express* 11 = 1 x16 PCI Express* CFG[7]: PEG Training: <ul style="list-style-type: none"> 1 = (default) PEG Train immediately following RESET# de assertion. 0 = PEG Wait for BIOS for training. CFG[19:8]: Reserved configuration lanes. | I/O | GTL | SE | All processor lines. CFG[2], CFG[6:5] and CFG[7] are relevant for H and S-processor line only and test point may be placed on the board for them. |

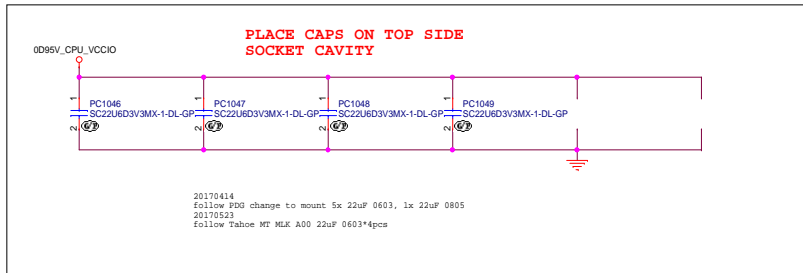
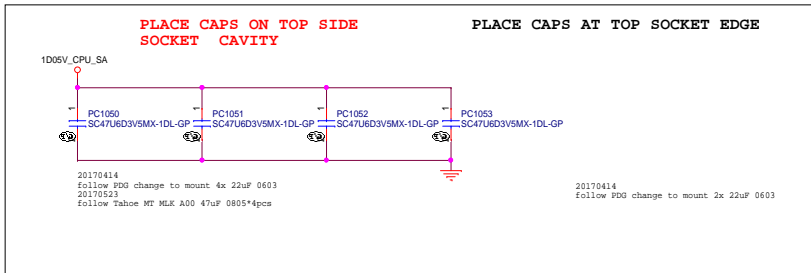
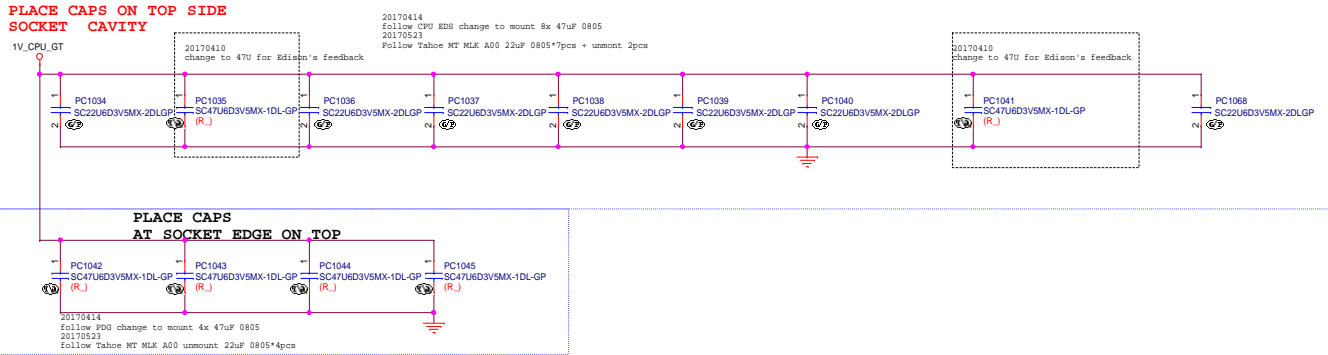


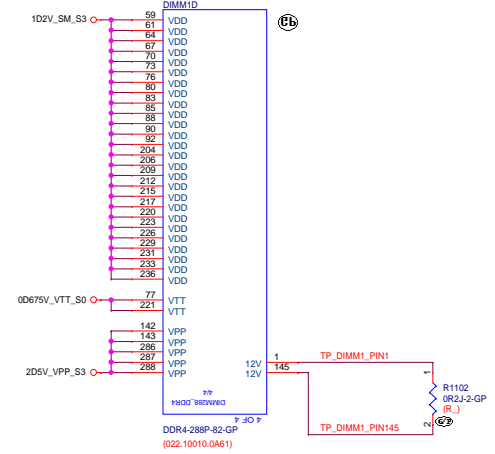
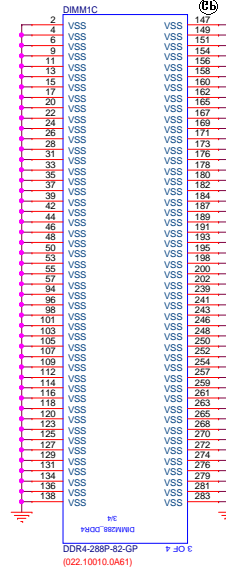
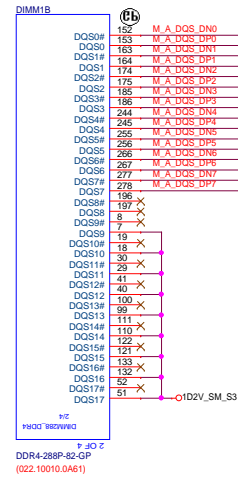






Follow D9 22uF*7 2017/08/23



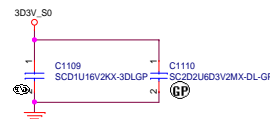
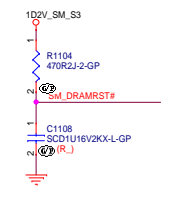
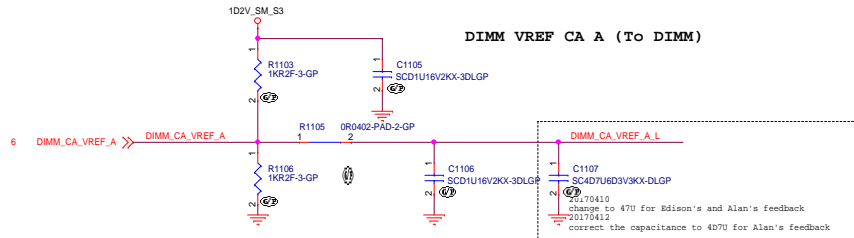


DIMM VREF DQ A (To DIMM/CPU)


Del for DDR4 Modify

Del C82, C83


For DDR4 Modify



| | | | | |
|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |

| | | |
|---|--|---|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. |
| Title Reserved | | |
| Size A | Document Number Gambit MLK MT/Eagle MT CFL | Rev A00 |
| Date: Friday, February 02, 2018 | Sheet 13 of 107 | |

| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

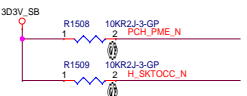
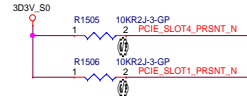
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| Title <div>Reserved</div> | |
| Size A | Document Number Gambit MLK MT/Eagle MT CFL |
| Date: Friday, February 02, 2018 | |
| Sheet | 14 of 107 |
| Rev A00 | |

TP1501 1 TP_VSS_AL37

20170406
USB charger function is removed
net CNV_CLK_BK1 @ pin Y47
net PCH_CLK_CTL3 @ pin AA45 is removed

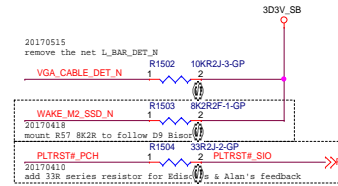
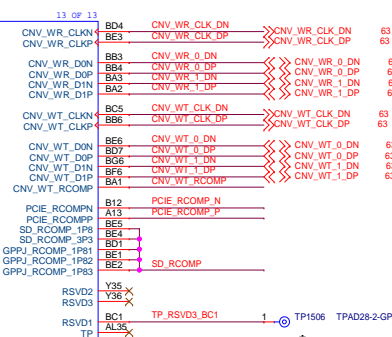
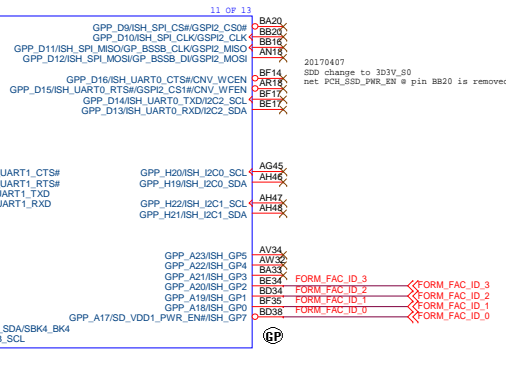
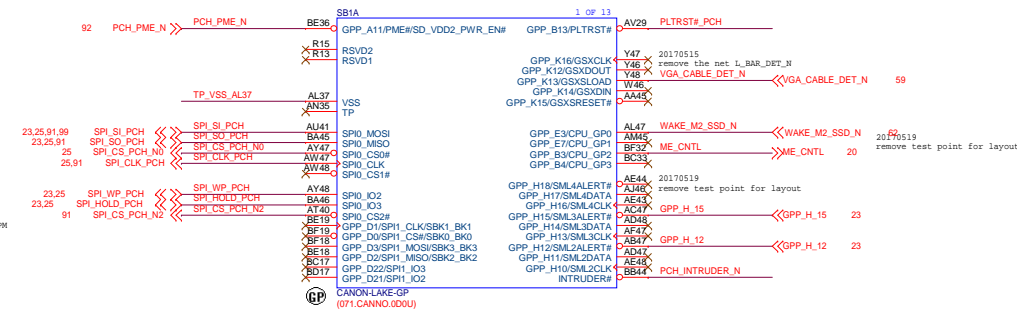
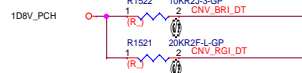
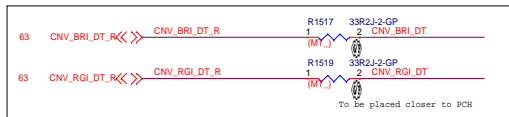
20170519
remove test point for layout

20170406
change to single 32MB SPI ROM
remove SPI_CS_PCH_N2
change SPI_CS_PCH_N1 to TFM
20170605
according to PDD, change SPI_CS_PCH_N2 to TFM
remove SPI_CS_PCH_N1

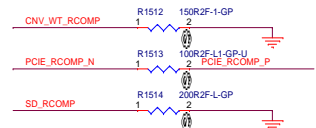
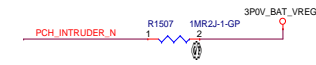


20170413
change to on board power switch
remove the net PP_CHL_DET @ pin BF8
20170420
add the net PP_CHL_DET back for SFF

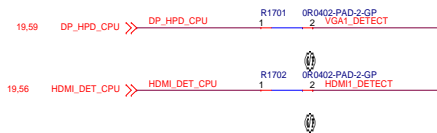
20170413
change to on board power switch
remove the net PP_CHL_DET @ pin BF8
20170420
add the net PP_CHL_DET back for SFF



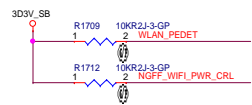
20170515
remove the net L_BAR_DET_N
20170418
mount B57 8K2R to follow D8 Bisc
20170410
add 33R series resistor for Edin
20170410
add 33R series resistor for Edin & Alan's feedback



DELL Wistron Corporation
21F, 88, Sec 1, Hsin Tai Wu Rd., Hsichih,
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20170413
change to on board power switch
remove the net CHASSIS_ID_0 @ pin L47
20170420
add the net CHASSIS_ID_0 back for SFP

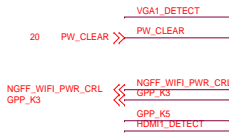


20170426
change to HSD

HSD4

HSD1

20170418
PW_CLEAR change from GPP_K9 to GPP_K10 to follow D9 Bison
PCH_RST_GPD change from GPP_K10 to GPP_P23 to follow D9 Bison



60 SATA_TX_PCH_N1

60 SATA_TX_PCH_P1

60 SATA_RX_PCH_N1

60 SATA_RX_PCH_P1

60 SATA_TX_PCH_N0

60 SATA_TX_PCH_P0

60 SATA_RX_PCH_N0

60 SATA_RX_PCH_P0

60 SATA_TX_PCH_N1

60 SATA_TX_PCH_P1

60 SATA_RX_PCH_N1

60 SATA_RX_PCH_P1

60 SATA_TX_PCH_N0

60 SATA_TX_PCH_P0

60 SATA_RX_PCH_N0

60 SATA_RX_PCH_P0

60 SATA_TX_PCH_N1

60 SATA_TX_PCH_P1

60 SATA_RX_PCH_N1

60 SATA_RX_PCH_P1

60 SATA_TX_PCH_N0

60 SATA_TX_PCH_P0

60 SATA_RX_PCH_N0

60 SATA_RX_PCH_P0

60 SATA_TX_PCH_N1

60 SATA_TX_PCH_P1

60 SATA_RX_PCH_N1

60 SATA_RX_PCH_P1

60 SATA_TX_PCH_N0

60 SATA_TX_PCH_P0

60 SATA_RX_PCH_N0

60 SATA_RX_PCH_P0

60 SATA_TX_PCH_N1

60 SATA_TX_PCH_P1

60 SATA_RX_PCH_N1

60 SATA_RX_PCH_P1

60 SATA_TX_PCH_N0

60 SATA_TX_PCH_P0

60 SATA_RX_PCH_N0

60 SATA_RX_PCH_P0

SBIC

3 OF 13

AR2 CL_CLK

AT5 CL_DATA

AD4 CL_RST#

P48 GPP_K8

V48 GPP_K9

W47 GPP_K10

L47 GPP_K0

L48 GPP_K1

U47 GPP_K2

N48 GPP_K3

N47 GPP_K4

P47 GPP_K5

R46 GPP_K6

C36 PCIE11_TXPISATA0A_TXP

B36 PCIE11_TXNSATA0A_TXN

F39 PCIE11_RXPISATA0A_RXP

G38 PCIE11_RXNSATA0A_RXN

AR42 GPP_F10SATA_SCLOCK

AD47 GPP_F11SATA_SLOAD

AD46 GPP_F12SATA_SDATAOUT0

C38 PCIE14_TXNSATA1B_TXN

D39 PCIE14_TXPISATA1B_TXP

D46 PCIE14_RXNSATA1B_RXN

C47 PCIE14_RXPISATA1B_RXP

B38 PCIE13_TXNSATA0B_TXN

C38 PCIE13_TXPISATA0B_TXP

C38 PCIE13_RXNSATA0B_RXN

C46 PCIE13_RXPISATA0B_RXP

E37 PCIE12_TXNSATA1A_TXP

D38 PCIE12_TXPISATA1A_TXP

L41 PCIE12_RXNSATA1A_RXN

H42 PCIE12_RXPISATA1A_RXP

B44 PCIE20_TXPISATA7_TXP

A44 PCIE20_TXNSATA7_TXN

R37 PCIE20_RXPISATA7_RXP

R36 PCIE20_RXNSATA7_RXN

D43 PCIE19_TXPISATA6_TXP

C44 PCIE19_TXNSATA6_TXN

N42 PCIE19_RXPISATA6_RXP

M44 PCIE19_RXNSATA6_RXN

GP CANON-LAKE-GP

(071.CANNO.000)

20170420

change PCIE1 slot port from PCIE10 to PCIE9

G36 PCIE_RX_PCH_N9

F36 PCIE_RX_PCH_P9

C34 PCIE_TX_PCH_N9

D34 PCIE_TX_PCH_P9

K37 PCIE10_RXN

J37 PCIE10_RXP

C35 PCIE10_TXN

B35 PCIE10_TXP

F44 SATA_RX_PCH_N2

E45 SATA_RX_PCH_P2

B40 SATA_TX_PCH_N2

C40 SATA_TX_PCH_P2

L41 SATA_RX_PCH_N3

M40 SATA_RX_PCH_P3

B41 SATA_TX_PCH_N3

C41 SATA_TX_PCH_P3

K43 PCIE17_RXNSATA4_RXN

K44 PCIE17_RXPISATA4_RXP

A42 PCIE17_TXNSATA4_TXN

B42 PCIE17_TXPISATA4_TXP

P41 PCIE18_RXNSATA5_RXN

R40 PCIE18_RXPISATA5_RXP

C42 PCIE18_TXNSATA5_TXN

D42 PCIE18_TXPISATA5_TXP

AK48 GPP_E8SATA_LED0

AK47 GPP_E1SATA_PCIE1SATA0P1

AK47 GPP_E2SATA_PCIE2SATA0P2

AK47 GPP_F0SATA_PCIE3SATA0P3

AK47 GPP_F1SATA_PCIE4SATA0P4

AK47 GPP_F2SATA_PCIE5SATA0P5

AK47 GPP_F3SATA_PCIE6SATA0P6

AK47 GPP_F4SATA_PCIE7SATA0P7

AK47 GPP_F21EDP_BKLTCTL

AK47 GPP_F20EDP_BKLTEN

AK47 GPP_F19EDP_VDDEN

AD3 THERMTRIP#_PCH

AF2 PCH_PECI

AF3 PM_SYNC_PCH

AG5 PLTRST_CPU_N

AE2 PM_DOWN_PCH

4.99

4

62

62

62

62

62

62

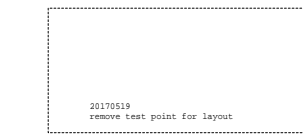
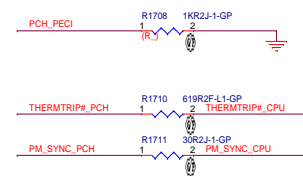
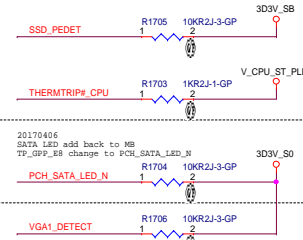
62

62

PCIE1 slot

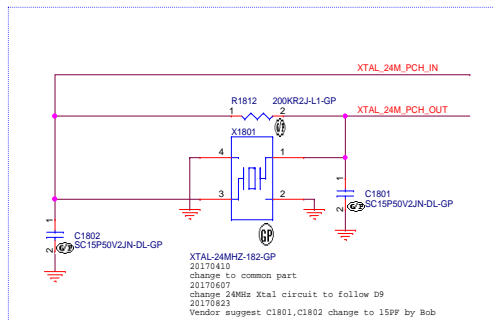
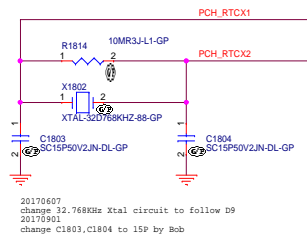
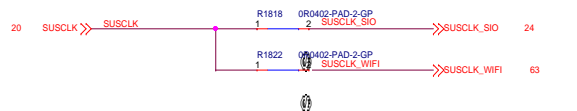
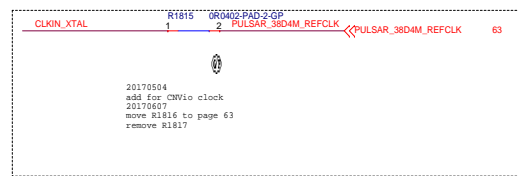
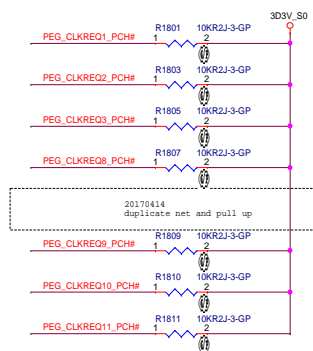
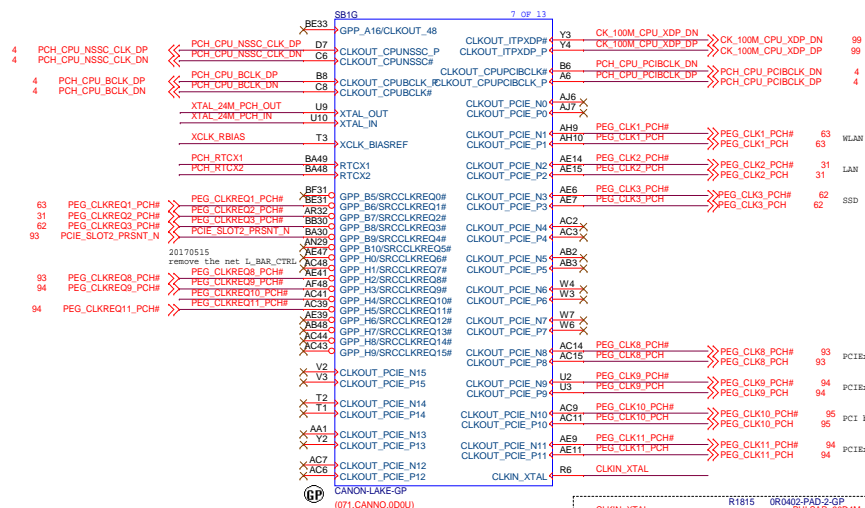
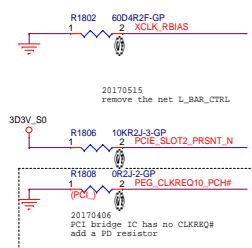
20170426
change to ODD

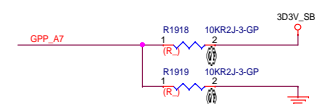
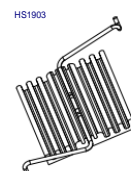
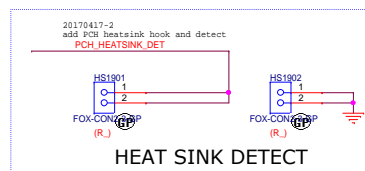
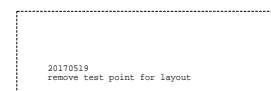
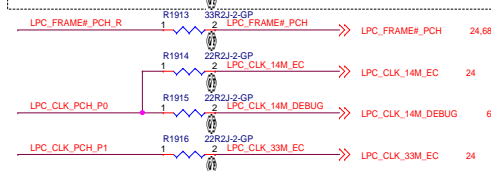
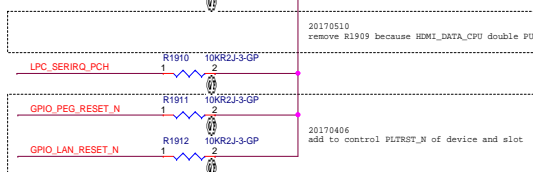
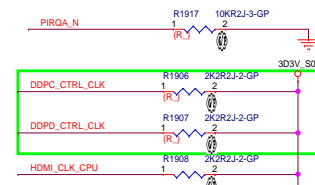
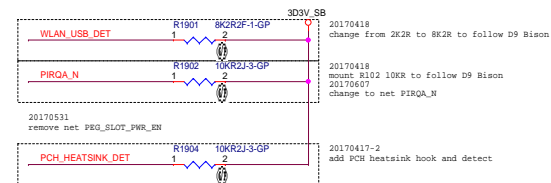
HSD3

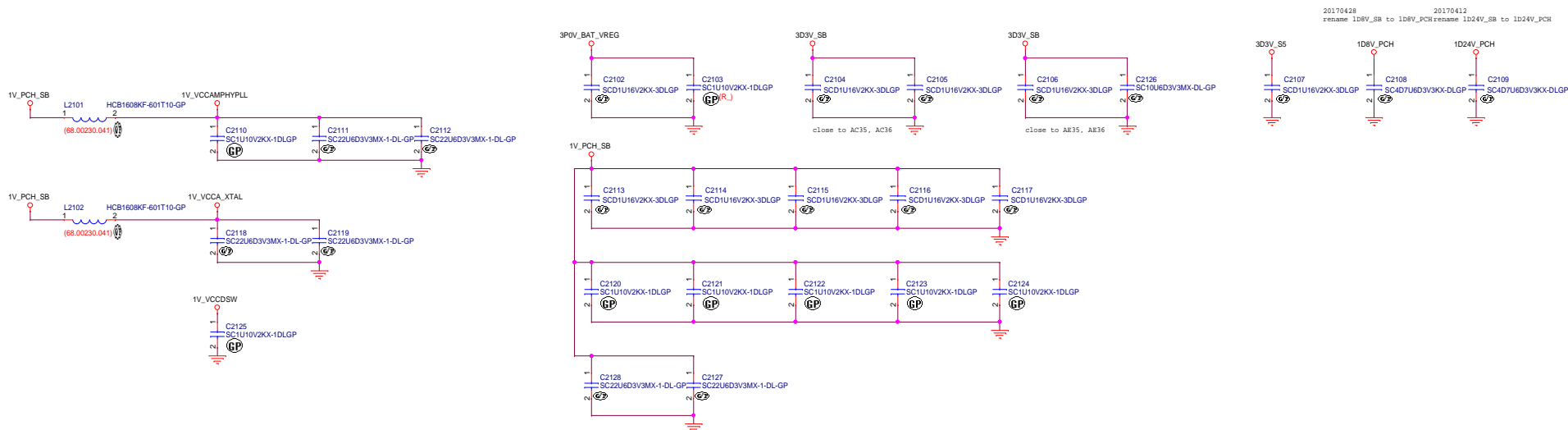


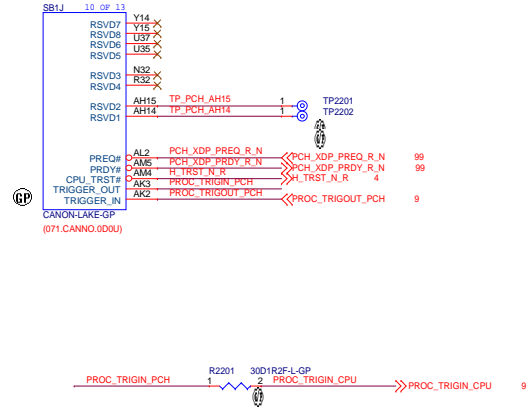
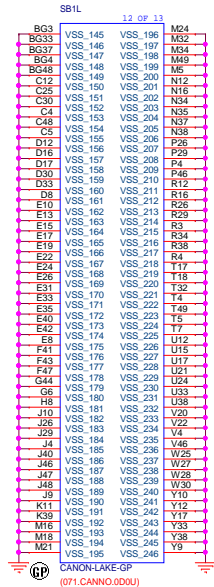
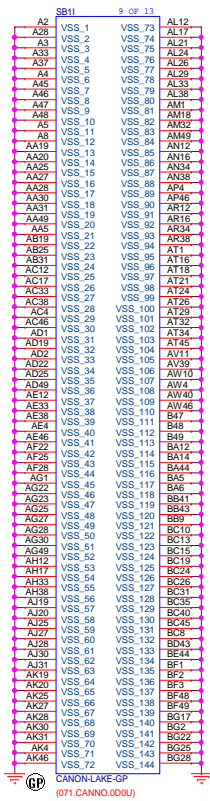
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taippei Hsien 221, Taiwan, R.O.C.

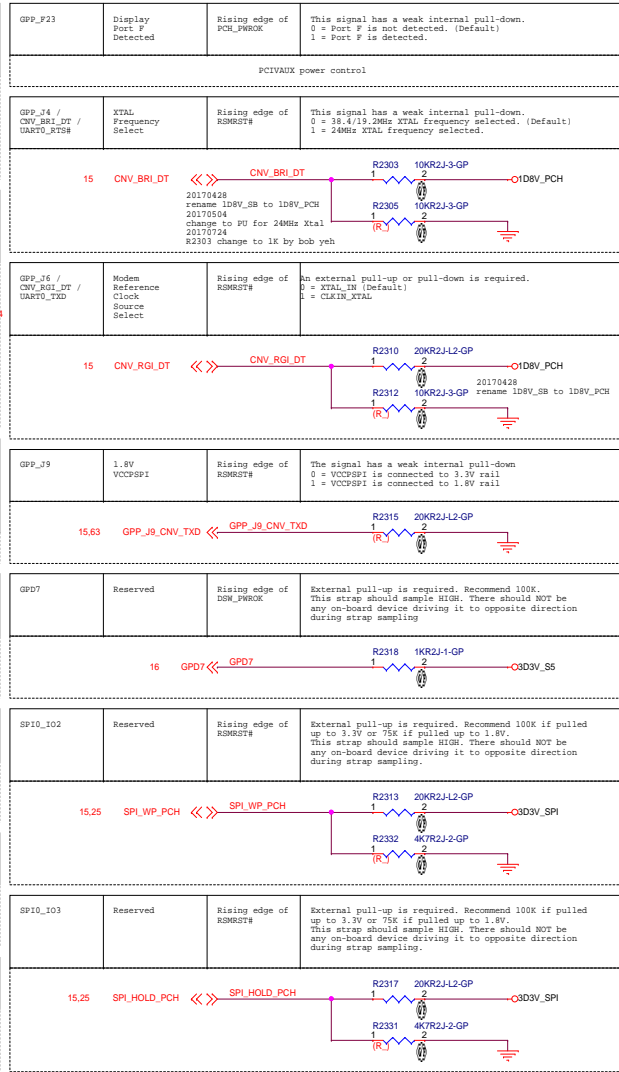
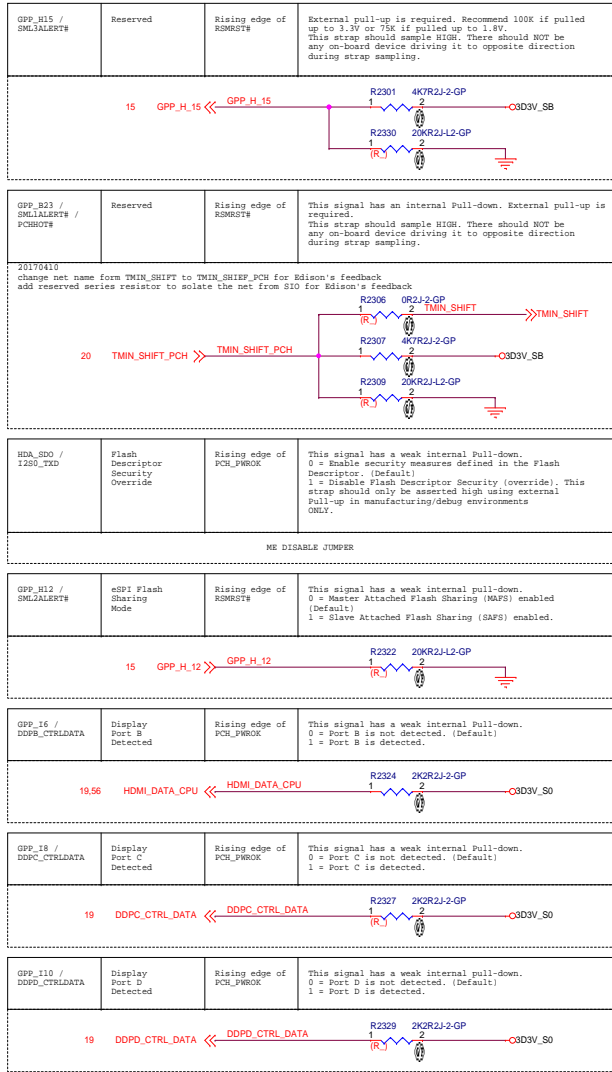
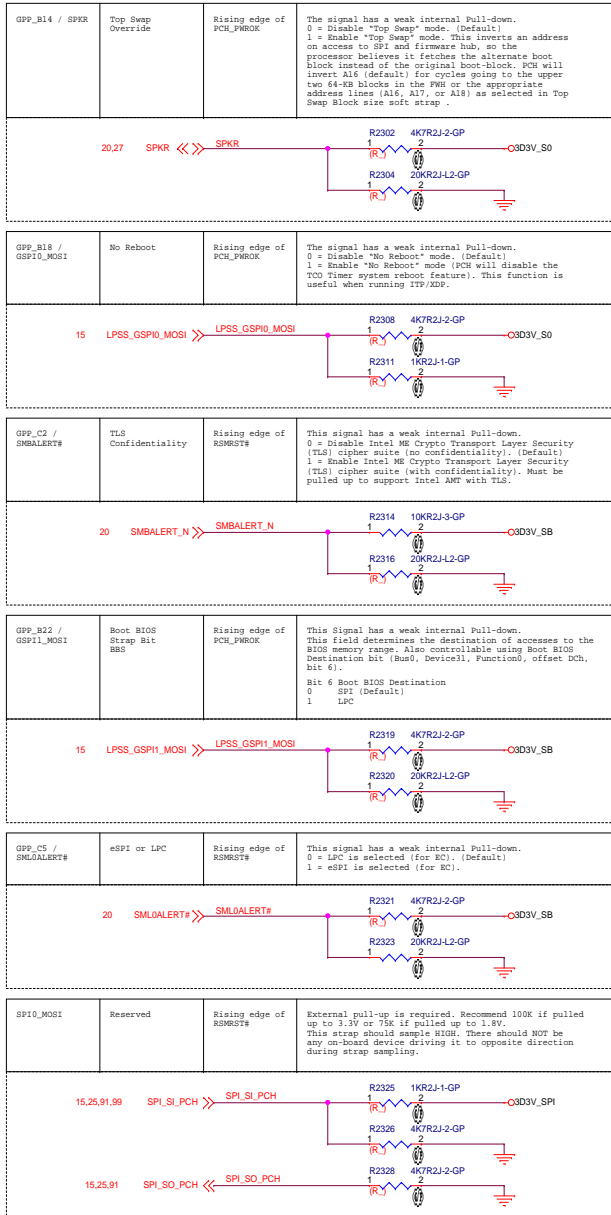
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| File | PCH (PCI-E/SATA) | | |
| Size | Document Number | Rev | |
| C | Gambit MLK MT/Eagle MT CFL | A00 | |
| Date: | Friday, February 02, 2018 | Sheet | 17 of 107 |

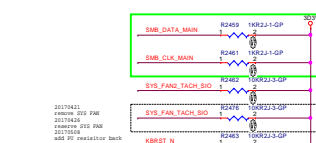
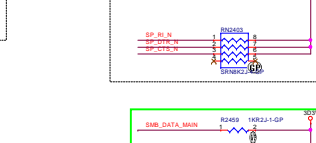
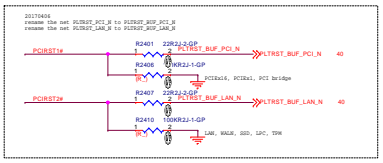
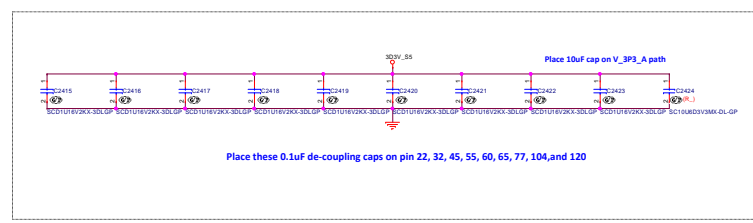




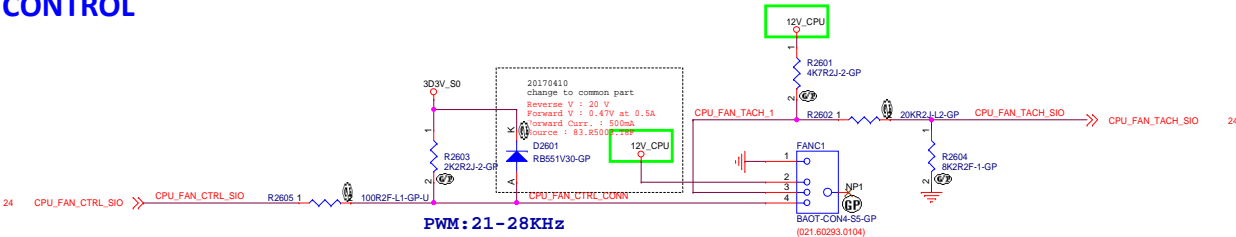






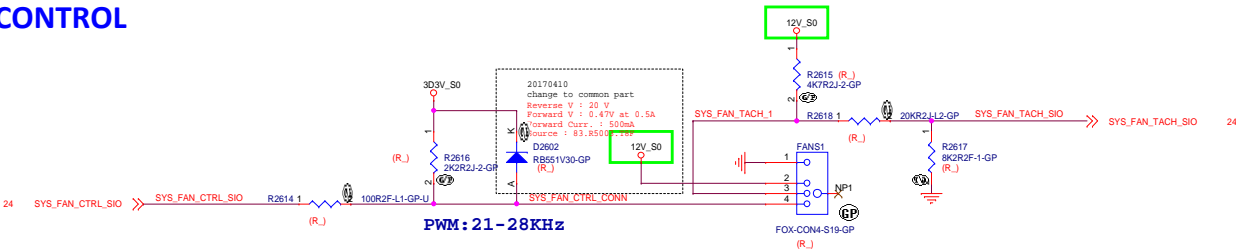
[illegible]

CPU FAN CONTROL



SYS FAN CONTROL

20170421
remove SYS FAN
20170424
reserve SYS FAN



Thermal sensor G709

20170413
change thermal shut down solution

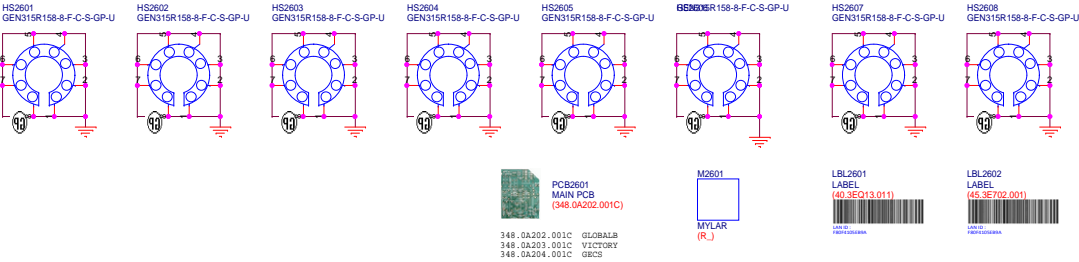
$R_{SET} (k\Omega) = 0.0012T^2 - 0.9308T + 96.147$

| | |
|--------|-------------|
| Temp.= | 108 °C |
| RSET= | 9.6174 Kohm |

| | |
|------------|--------------------|
| G709 | |
| HYST = VCC | Hysterisis is 10°C |
| HYST = GND | Hysterisis is 2°C |

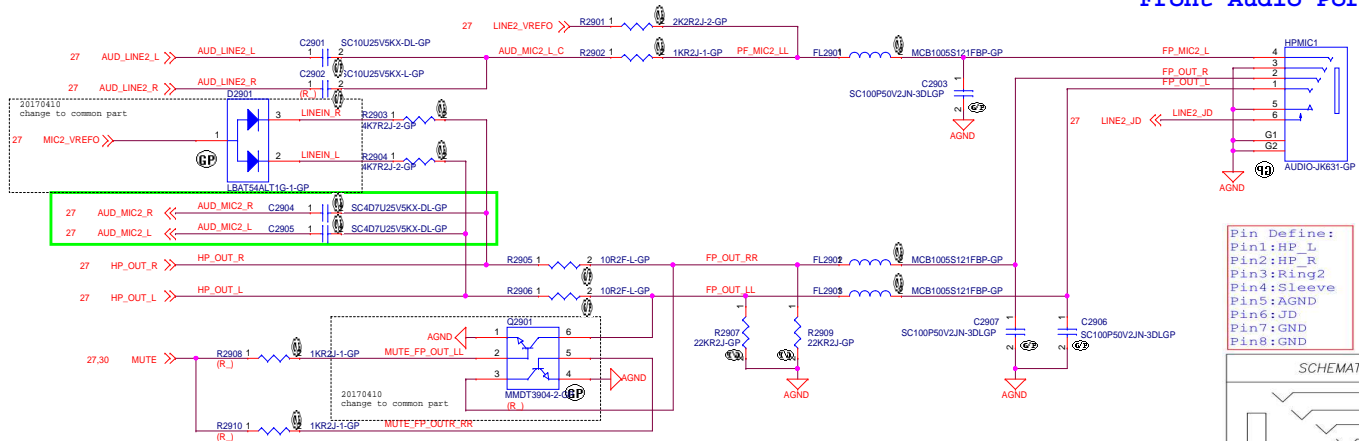
Modify circuit for thermal shutdown issue

20170524
recall the symbol of the screw holes

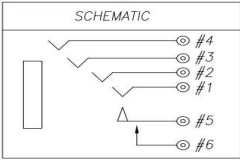


20170412
remove internal speaker amp

Front Audio Port



Pin Define:
Pin1:HP_L
Pin2:HP_R
Pin3:Ring2
Pin4:Sleeve
Pin5:AGND
Pin6:JD
Pin7:GND
Pin8:GND

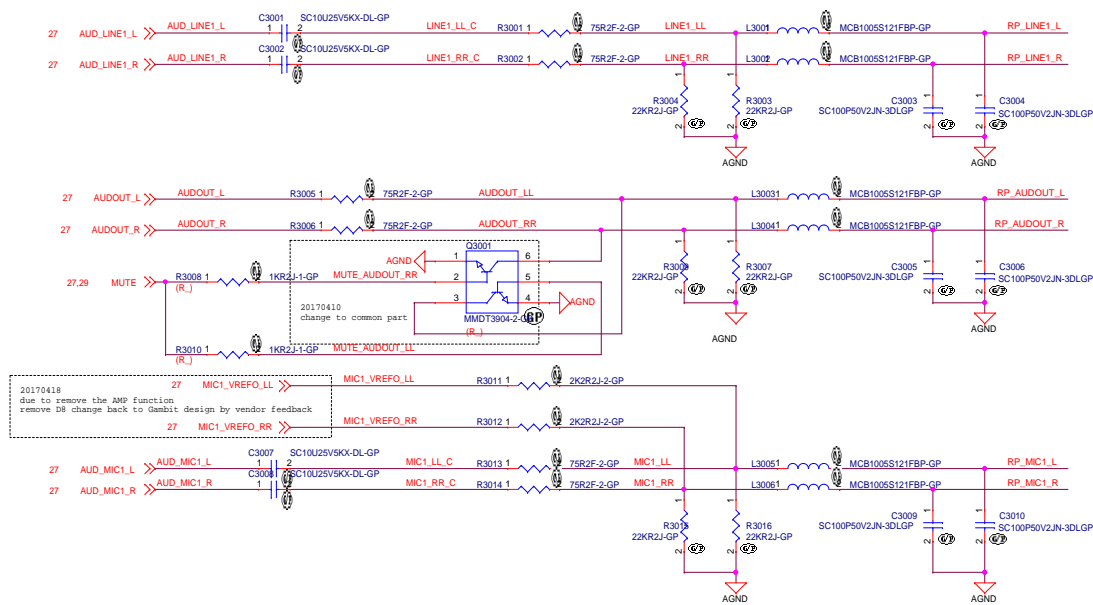


4-pin 3.5mm Headset Connector Pinout

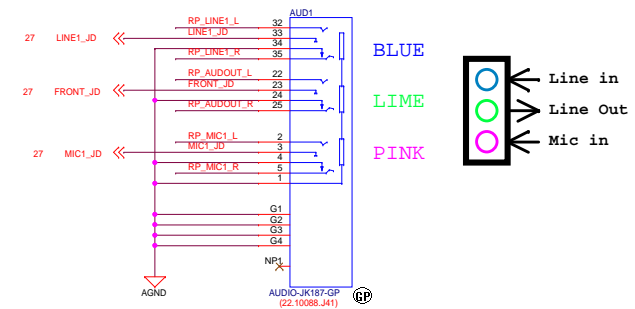


| Nokia, Lenovo mobile | | |
|----------------------|----------|-----------------|
| Pin Number | Pin Name | Description |
| 1 | Tip | Left Audio Out |
| 2 | Ring-1 | Right Audio Out |
| 3 | Ring-2 | Microphone |
| 4 | Sleeve | Ground / Common |

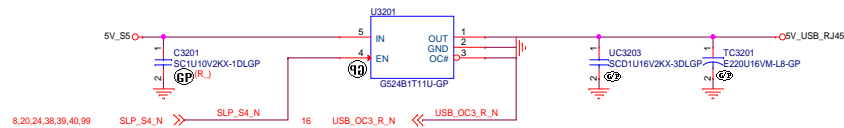
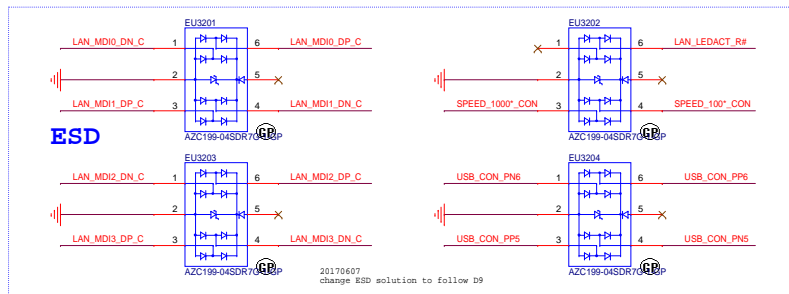
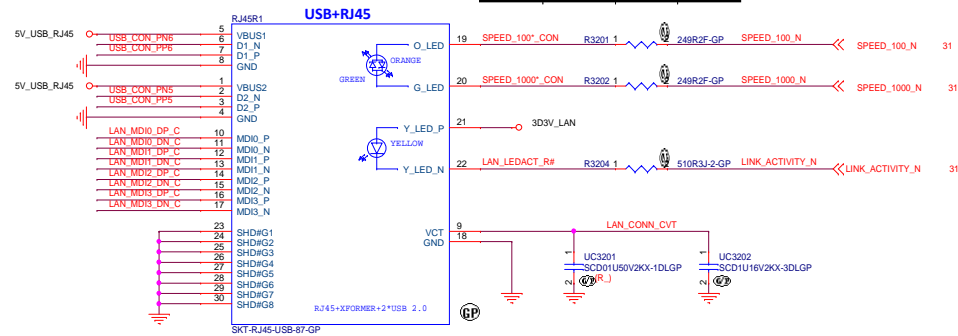
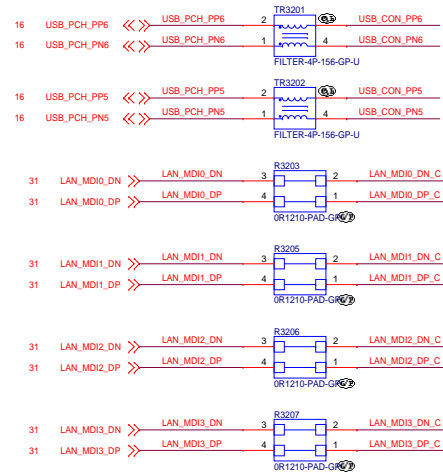
| iPhone, Samsung, Blackberry, HTC | | |
|----------------------------------|----------|-----------------|
| Pin Number | Pin Name | Description |
| 1 | Tip | Left Audio Out |
| 2 | Ring-1 | Right Audio Out |
| 3 | Ring-2 | Ground / Common |
| 4 | Sleeve | Microphone |

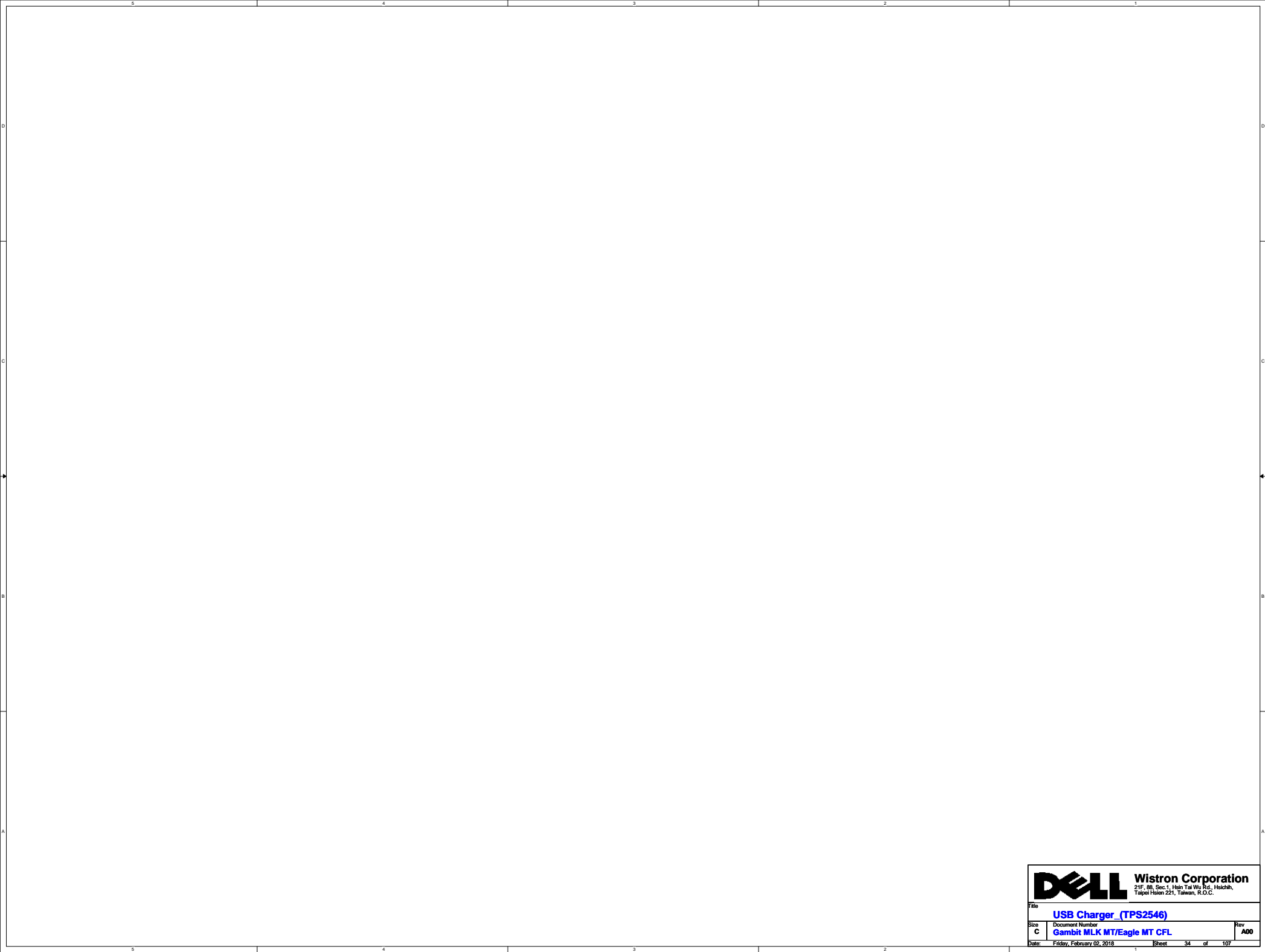



Rear Audio Port









| | | | |
|---|--|---|-------------------|
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title USB Charger (TPS2546) | | | |
| Size C | Document Number Gambit MLK MT/Eagle MT CFL | | Rev A00 |
| Date: Friday, February 02, 2018 | | Sheet | 34 of 107 |



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Taipei Hsien 221, Taiwan, R.O.C.

| Title |
|-------|
|-------|

Reserved

Size
B

| |
|-----------------|
| Document Number |
|-----------------|


Gambit MLK MT/Eagle MT CFL

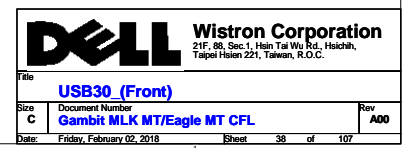
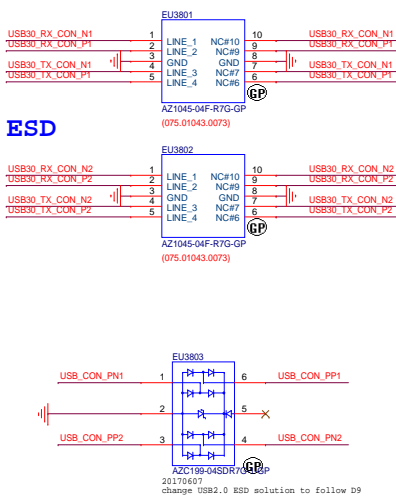
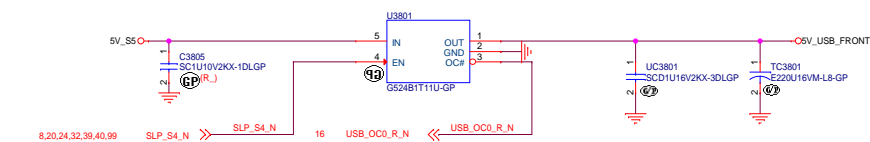
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| Rev | A00 |
|-----|-----|

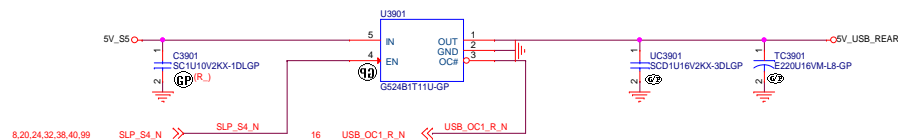
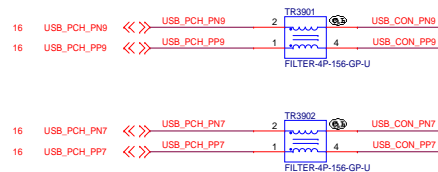
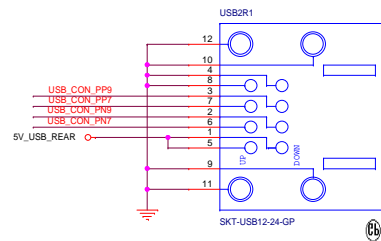
Date: Friday, February 02, 2018

Sheet 36 of 107

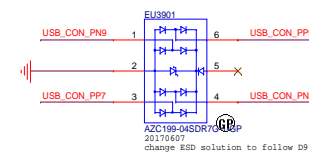
| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

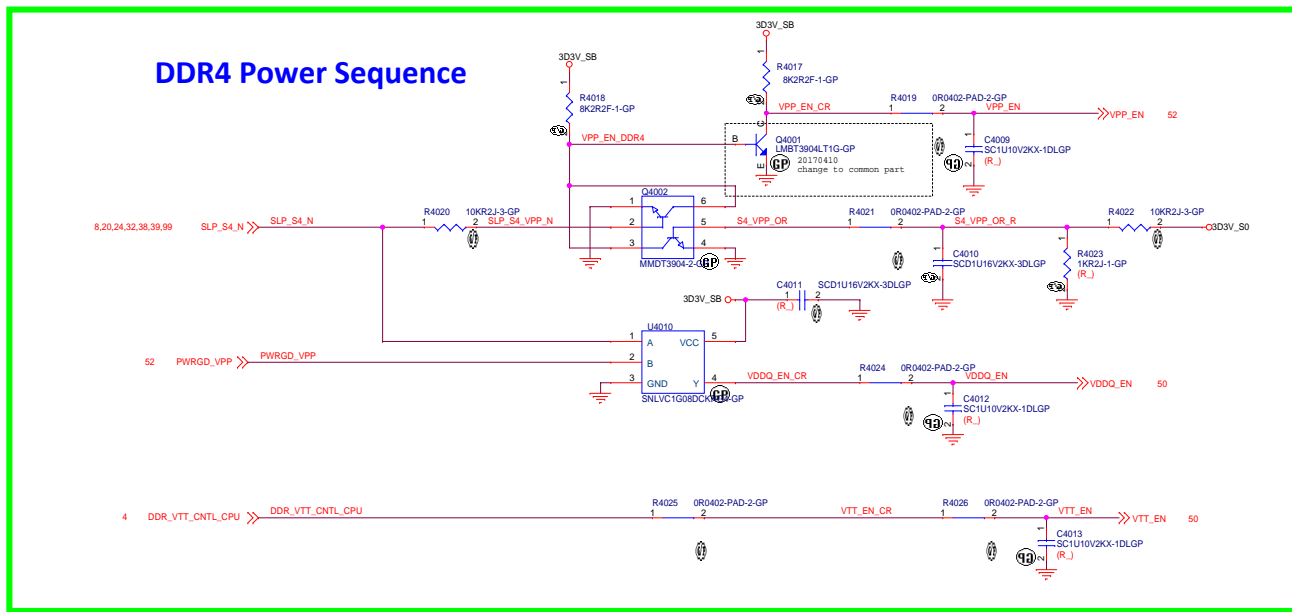
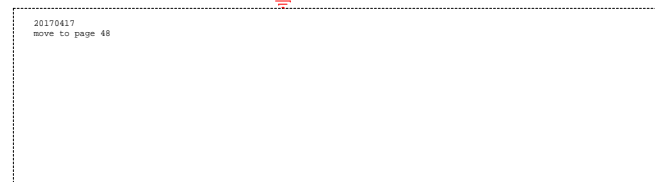
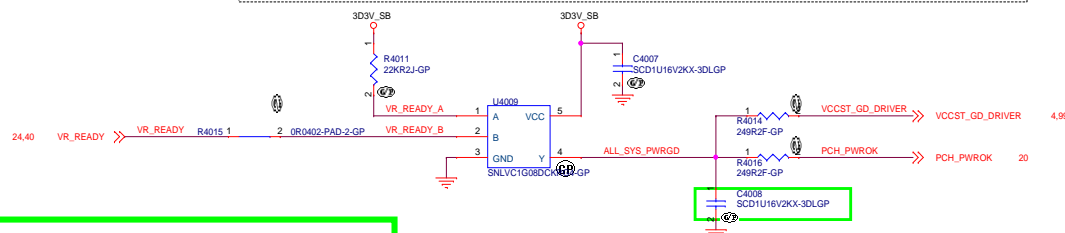
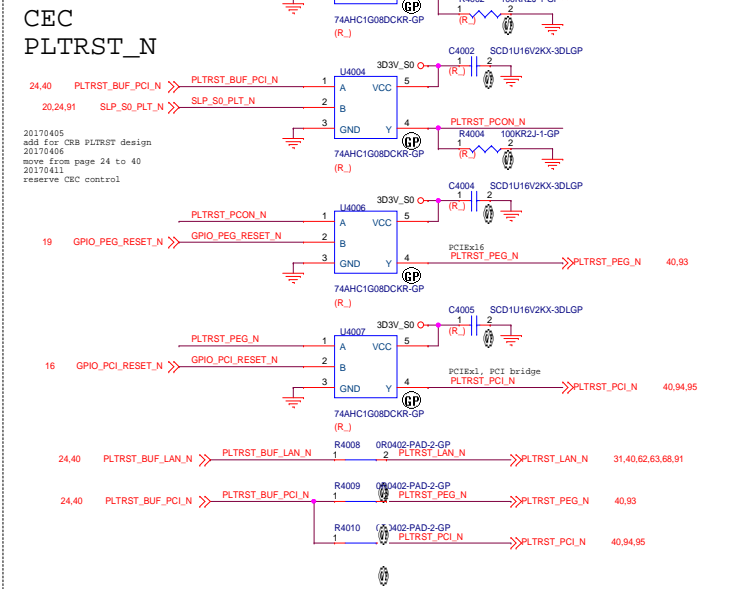
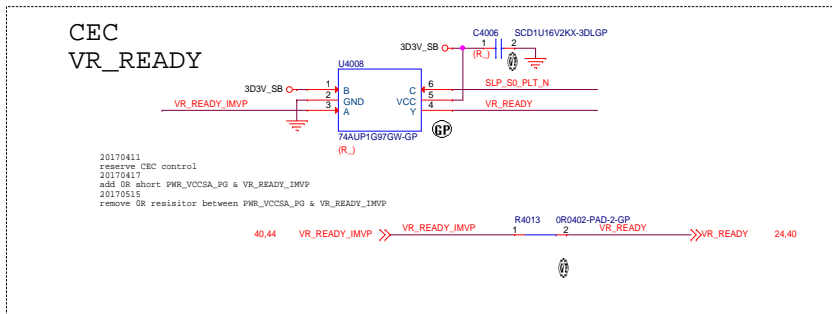
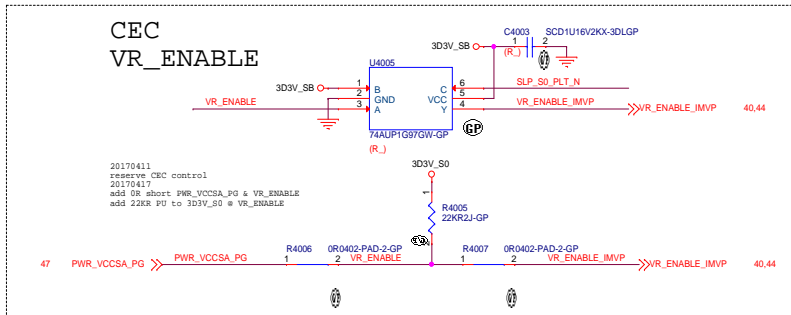
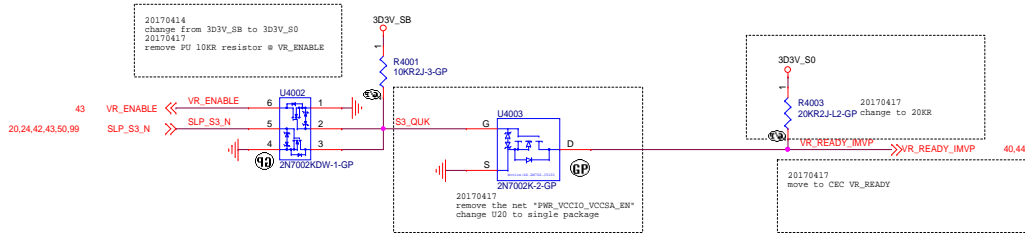
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|  <div> Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. </div> | |
| Title <div>Reserved</div> | |
| Size A | <div> Document Number Gambit MLK MT/Eagle MT CFL </div> |
| Date: Friday, February 02, 2018 | |
| Sheet 37 | of 107 |
| Rev A00 | |






ESD



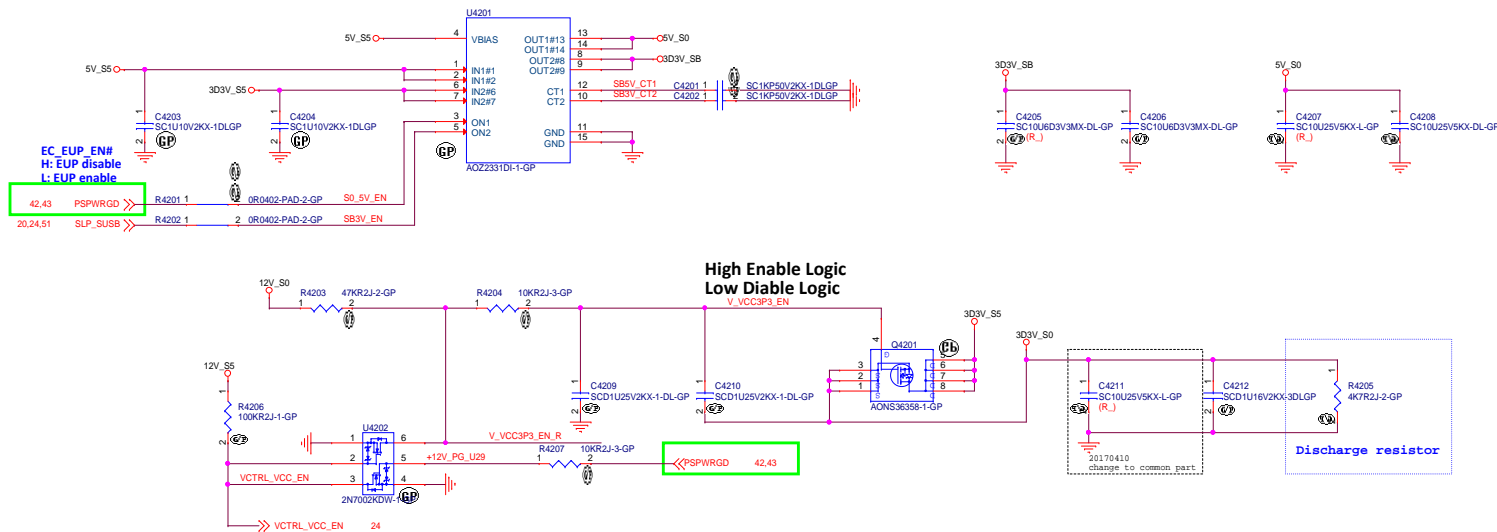


| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |



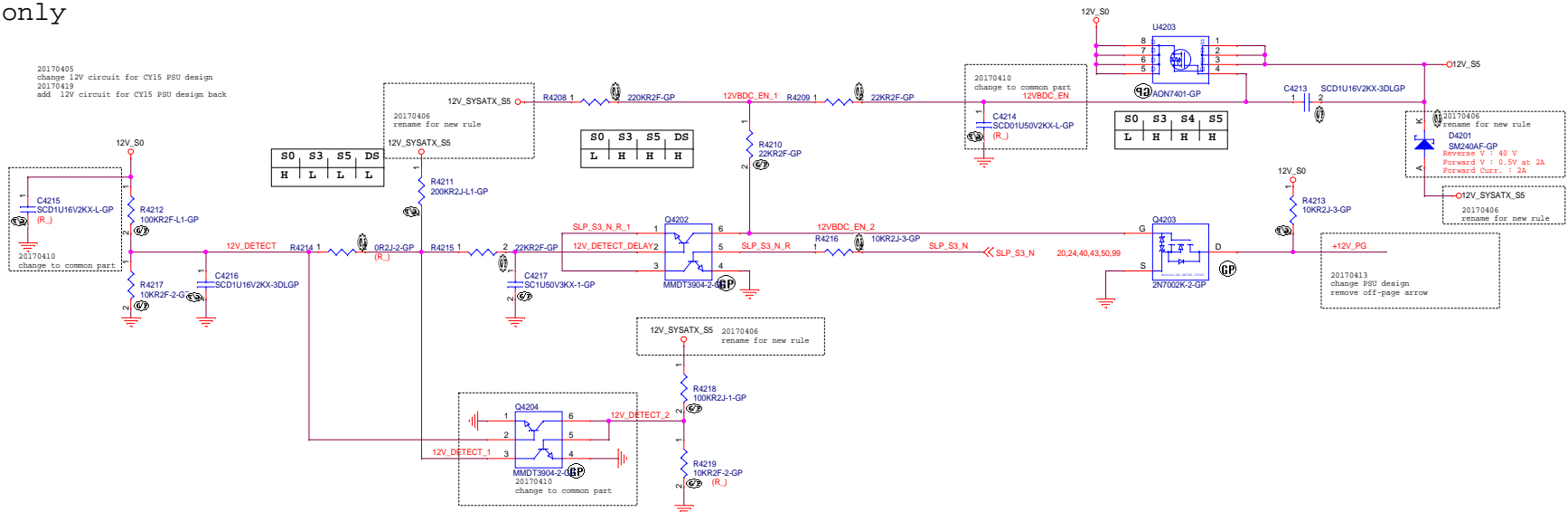
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 Taipei Hsien 221, Taiwan, R.O.C.

| | | |
|----------|----------------------------|-----------------|
| Title | | |
| Reserved | | |
| Size | Document Number | Rev |
| A | Gambit MLK MT/Eagle MT CFL | A00 |
| Date: | Friday, February 02, 2018 | Sheet 41 of 107 |



MT only

20170405
change 12V circuit for CY15 PSU design
20170419
add 12V circuit for CY15 PSU design back

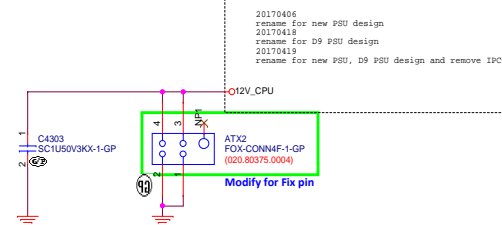




| | | | |
|---|-------|---|---------|
| 1 | PS_ON | 4 | P_OK |
| 2 | COM | 5 | +12VBDC |
| 3 | COM | 6 | +12VBDC |

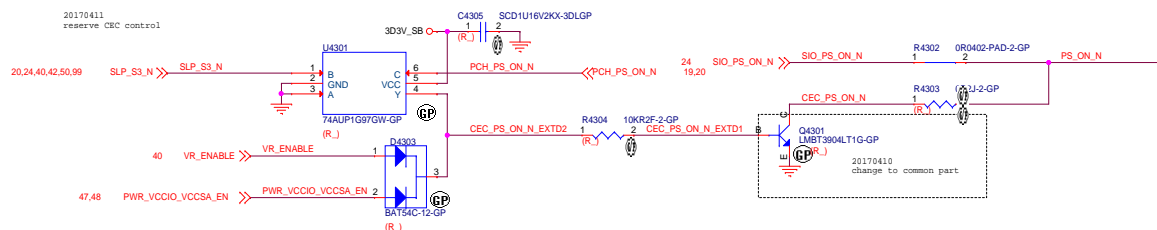
SFF only

20170417-2
change back to D9 PSU design
20170424
remove circuit for MT



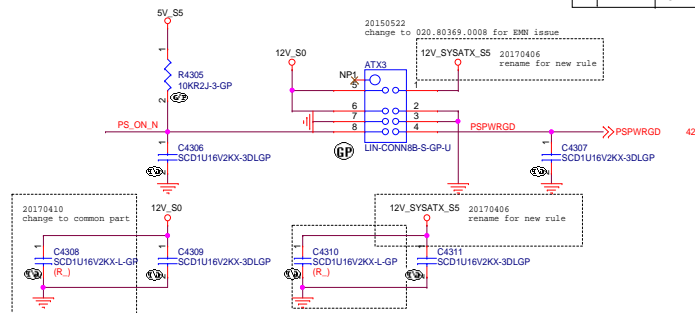
CEC PS_ON_N

20170411
reserve CEC control

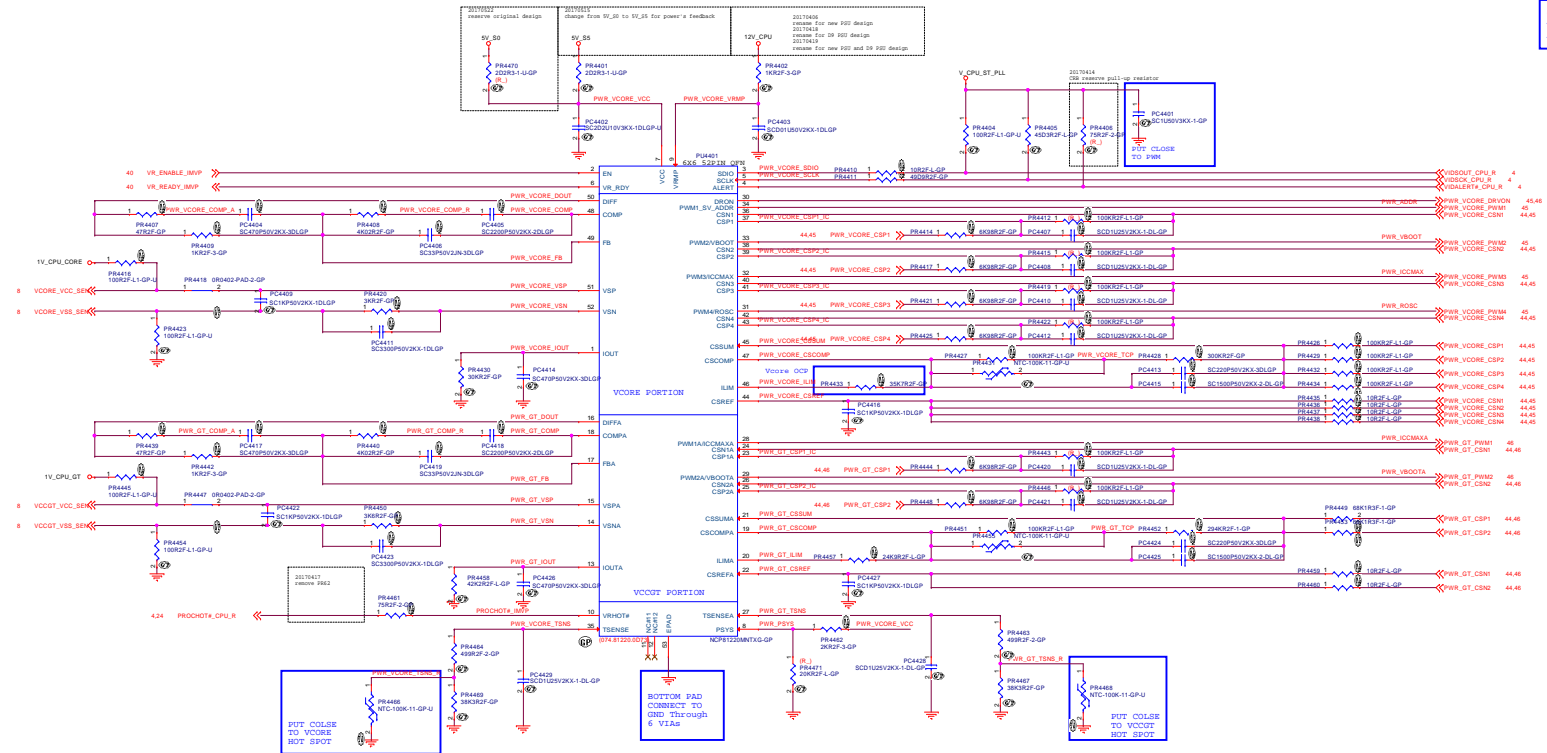


MT only

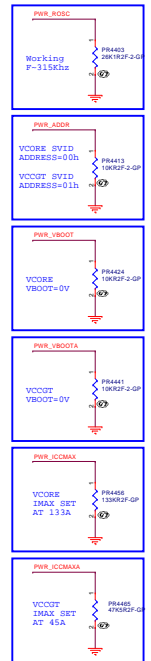
| | | | |
|---|--------|---|---------|
| 1 | +12VSB | 5 | +12VBDC |
| 2 | COM | 6 | +12VBDC |
| 3 | COM | 7 | COM |
| 4 | P_OK | 8 | PS_ON |

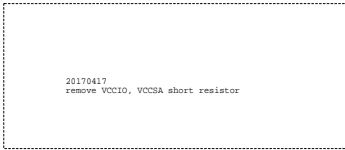


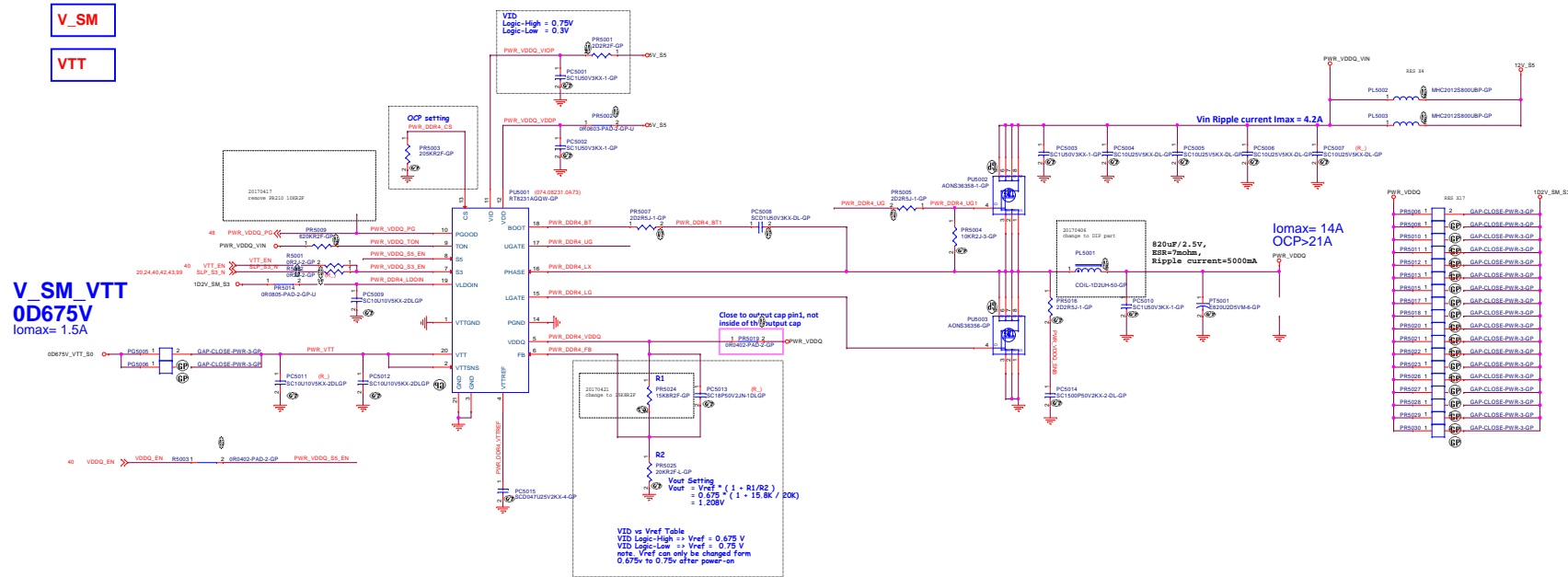
Intel Coffeelake IMVP8 POWER CKT - S-LINE 62 95W 4+2 PHASE

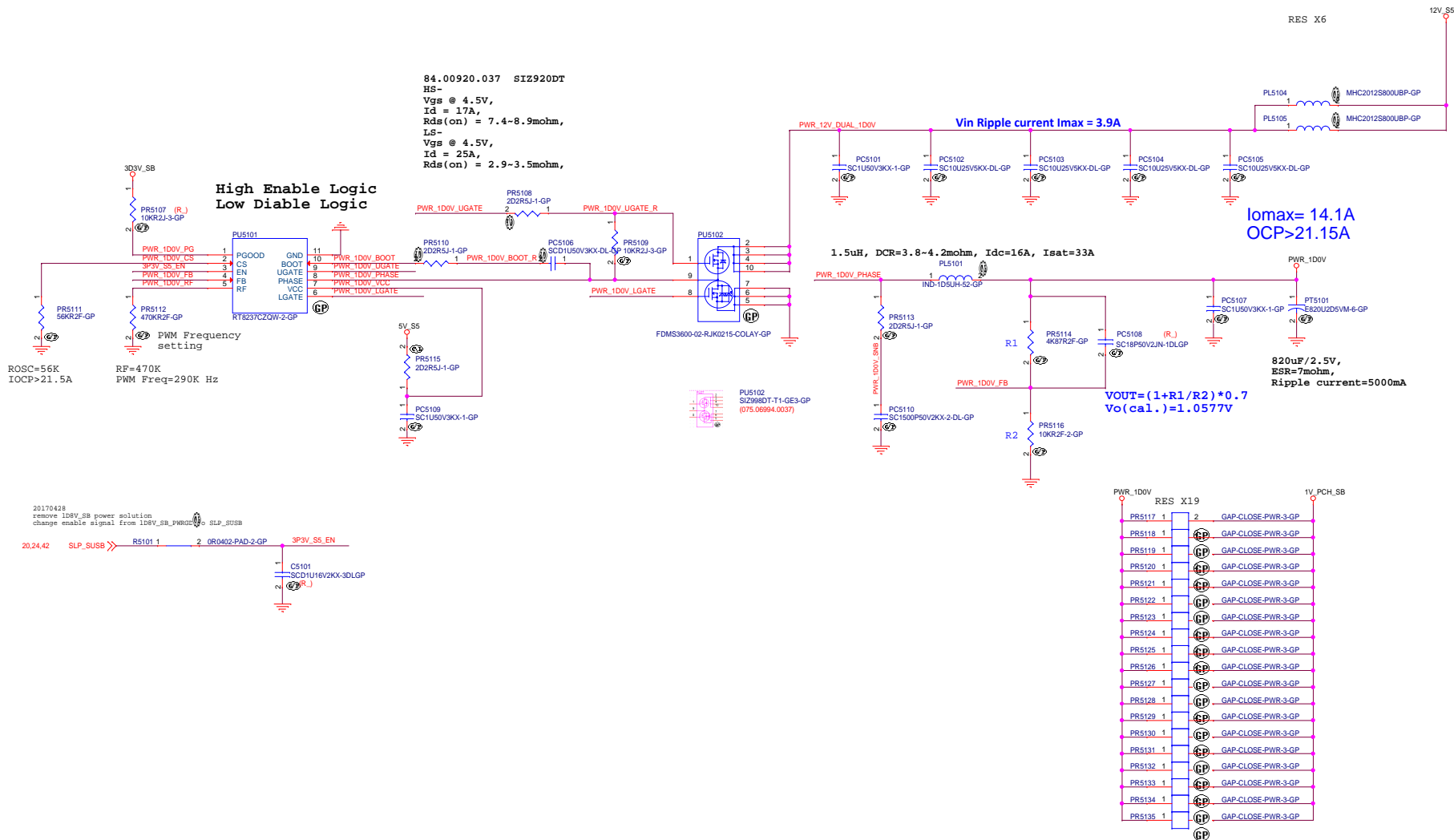


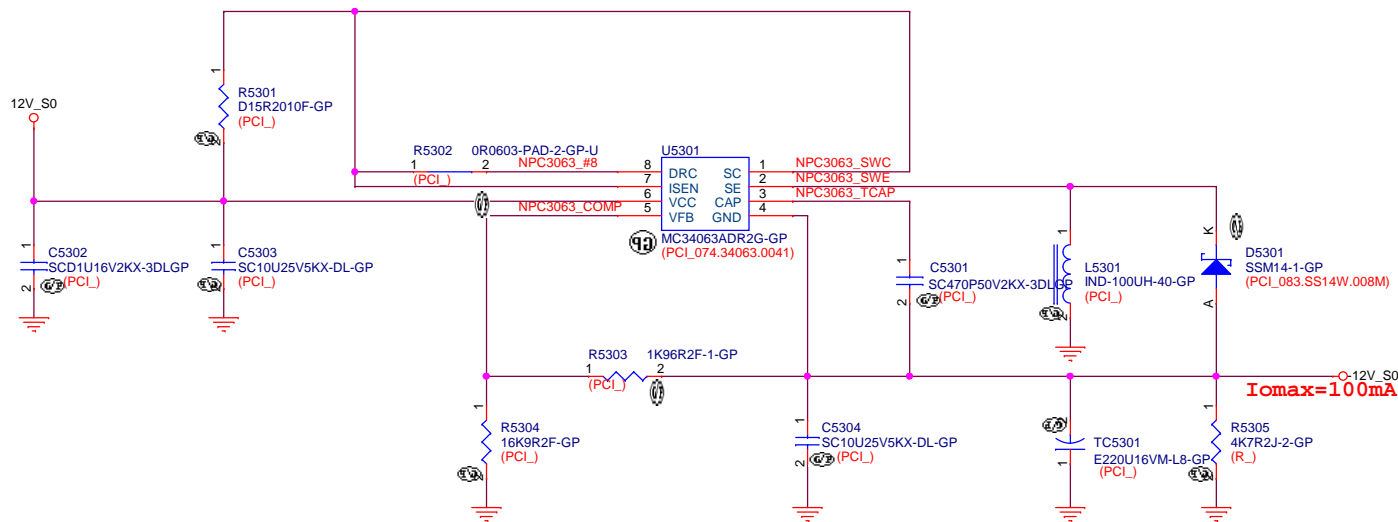
S-Line 62 65W CPU power spec
Vcore ICCMAX=133A, TDC=91A
VccGT ICCMAX=45A, TDC=30A












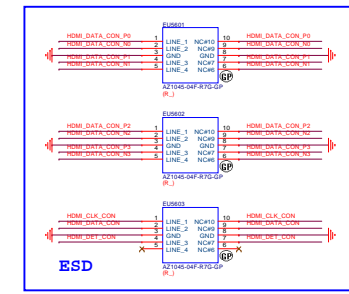
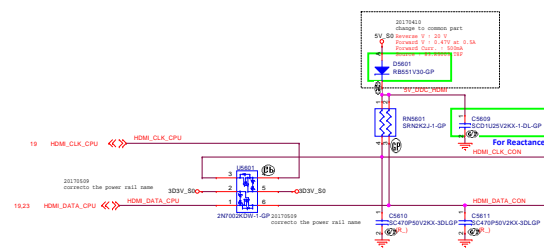
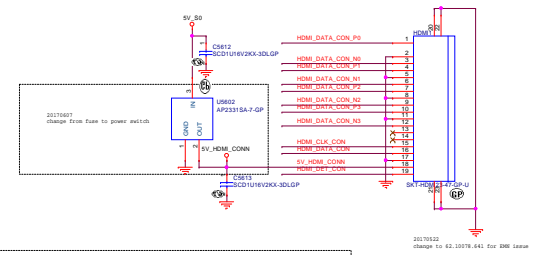
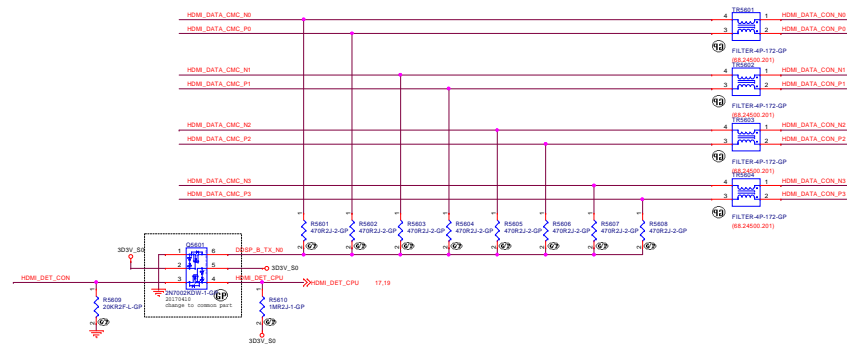
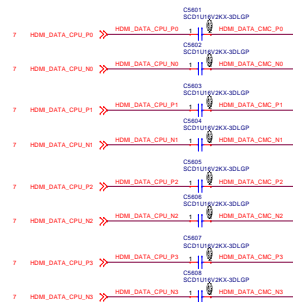
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| Title MINUS 12V (NCP3063) | |
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20170428
remove 1D8V_SB power solution


20170412
remove 1D24V_SB power solution

20170419
remove IPOC circuit


| | | | |
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| Title Reserve | | | |
| Size C | Document Number Gambit MLK MT/Eagle MT CFL | | Rev A00 |
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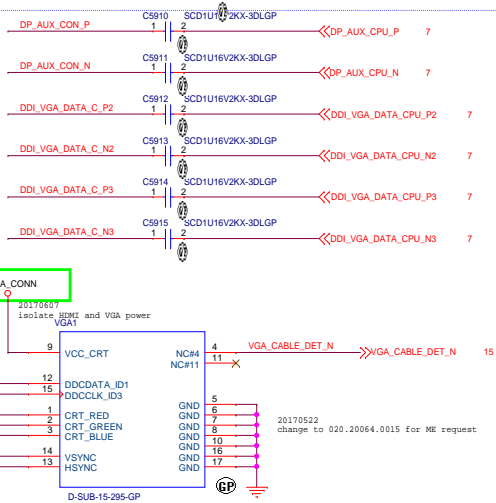
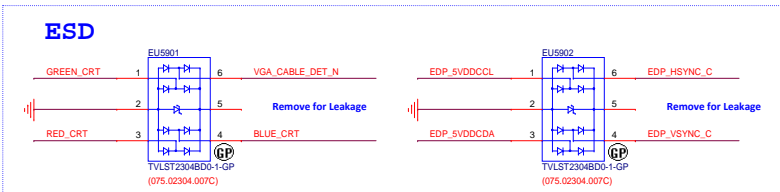
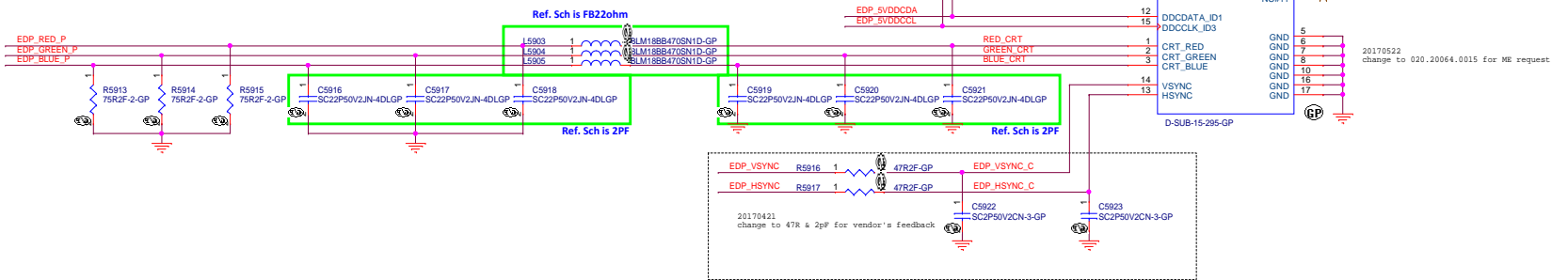
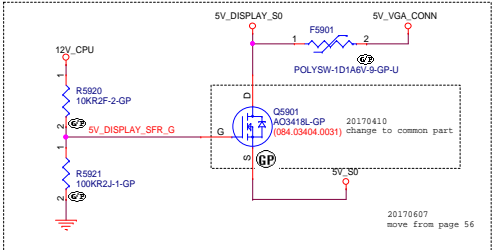


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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

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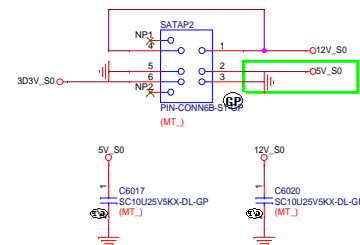
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|---|---|---|---|---|
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| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |

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2.5" SATA HDD POWER CONNECTOR
MT only



| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

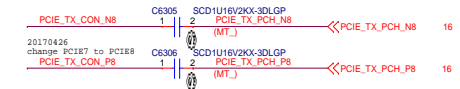
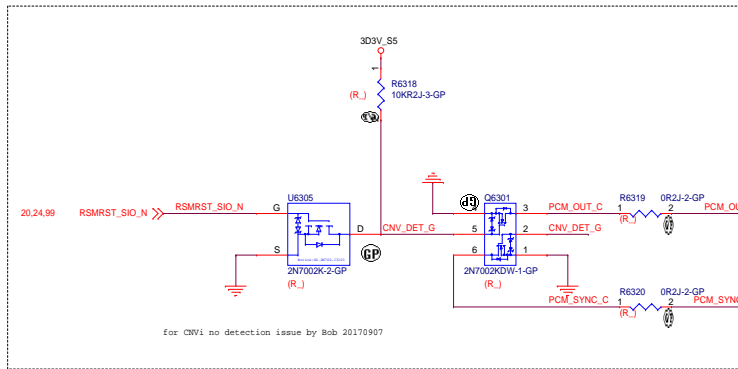
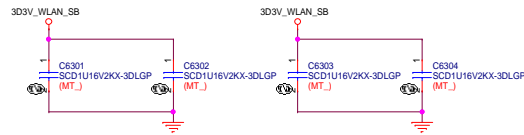


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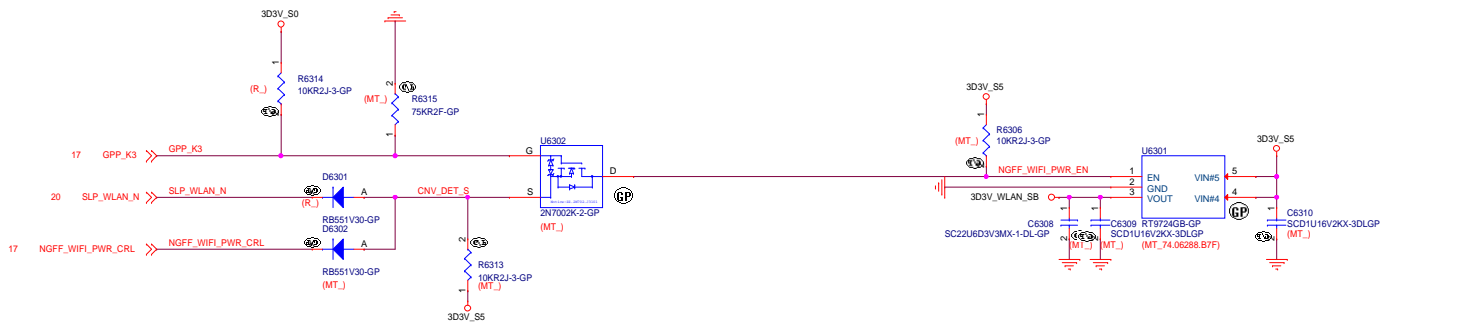
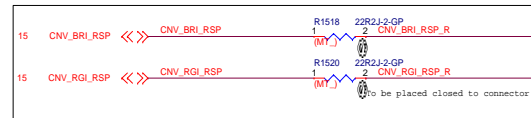
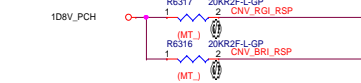
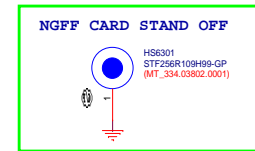
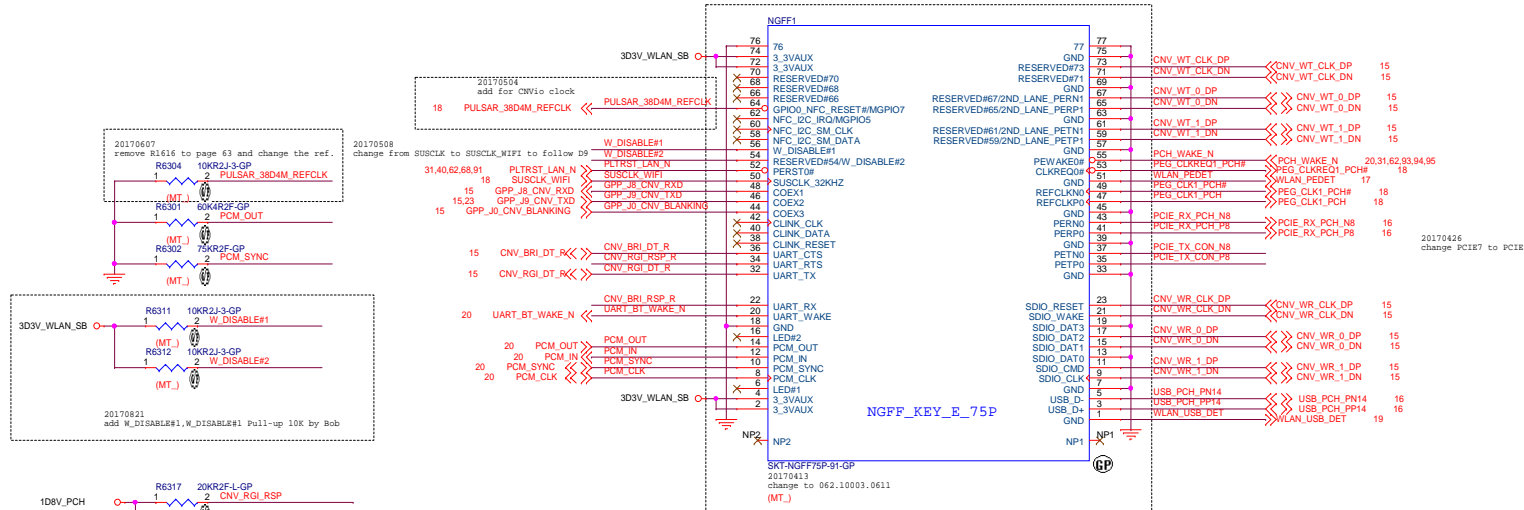
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| Title | | |
| Reserved | | |
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20170421
SSD change to PCIE21, 22, 23, 24 to support Optane





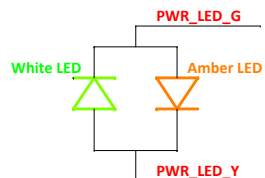
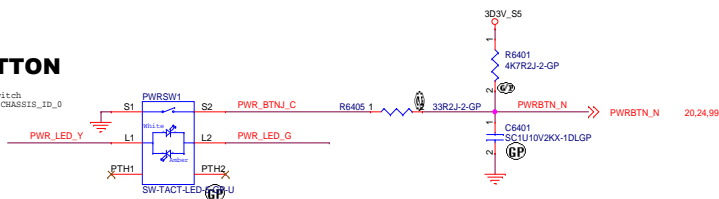
H: 4.2mm



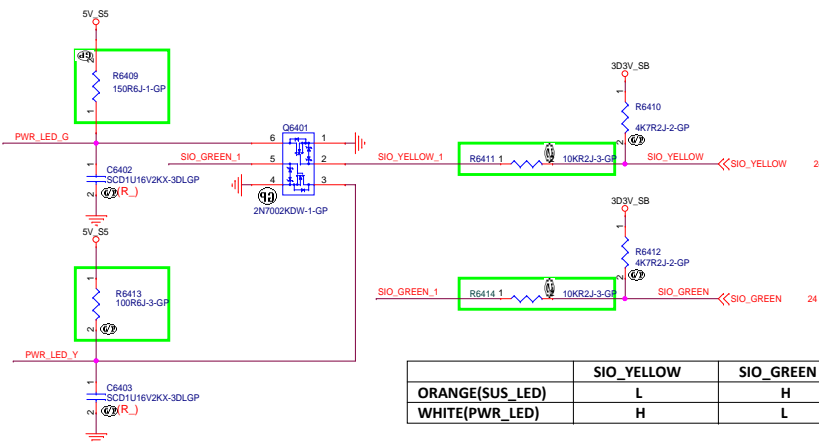
MT only

POWER BUTTON

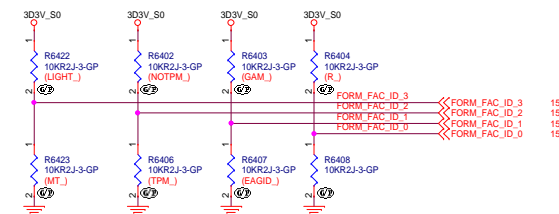
20170413
change to on board power switch
remove the net PP_CBL_DFT, CRASIS19_ID_0



| | |
|-----------------|-----------------|
| S0 | White |
| S3 | White(blinking) |
| S4/S5 | LED off |
| No Post | Amber |
| Failure to Post | Amber(blinking) |



| | SIO_YELLOW | SIO_GREEN |
|-----------------|------------|-----------|
| ORANGE(SUS_LED) | L | H |
| WHITE(PWR_LED) | H | L |



SKU ID

| Type | ID_3 | ID_2 | ID_1 | ID_0 |
|--------------------------------|------|------|------|------|
| Gambit MLK MT w/o TPM IC | 0 | 1 | 1 | 0 |
| Eagle MT w/ TPM IC | 0 | 0 | 0 | 0 |
| Eagle MT w/o TPM IC | 0 | 1 | 0 | 0 |
| Gambit MLK SFF w/o TPM IC | X | 1 | 1 | 1 |
| Eagle SFF w/ TPM IC | X | 0 | 0 | 1 |
| Eagle SFF w/o TPM IC | X | 1 | 0 | 1 |
| Eagle Light w/o TPM IC,M2,PCIe | 1 | 1 | 0 | 0 |

Chassis ID

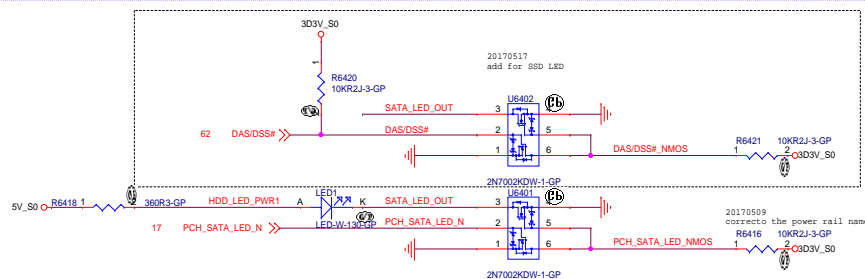
| ID_0 | Chassis | CY18 (CFL) | CY16 (KBL) |
|------|----------|------------|------------|
| 0 | Vostro | Eagle | Tahoe MLK |
| 1 | Inspiron | Gambit MLK | Gambit |

Power switch cable select

SFF only

POWER BUTTON


20170419
add back for SFF
20170424
remove circuit for MT




SFF only

20170410
change to mounted
20170424
remove circuit for MT


| | | | | | |
|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | |
| | | | | | |
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| | | | | | |
| | | | | | |
| D | | | | | D |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| C | | | | | C |
| | | | | | |
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| | | | | | |
| B | | | | | B |
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| | | | | | |
| A | | | | | A |
| 5 | 4 | 3 | 2 | 1 | |

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| Title Reserved | | | | | |
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| | | | | |
|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |

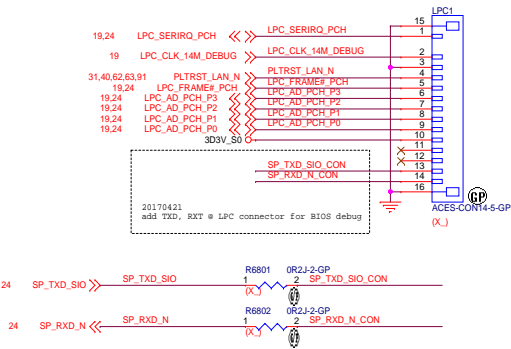
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|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |


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LPC DEBUG PORT

20170504
change to standard LPC debug connector




| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |



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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

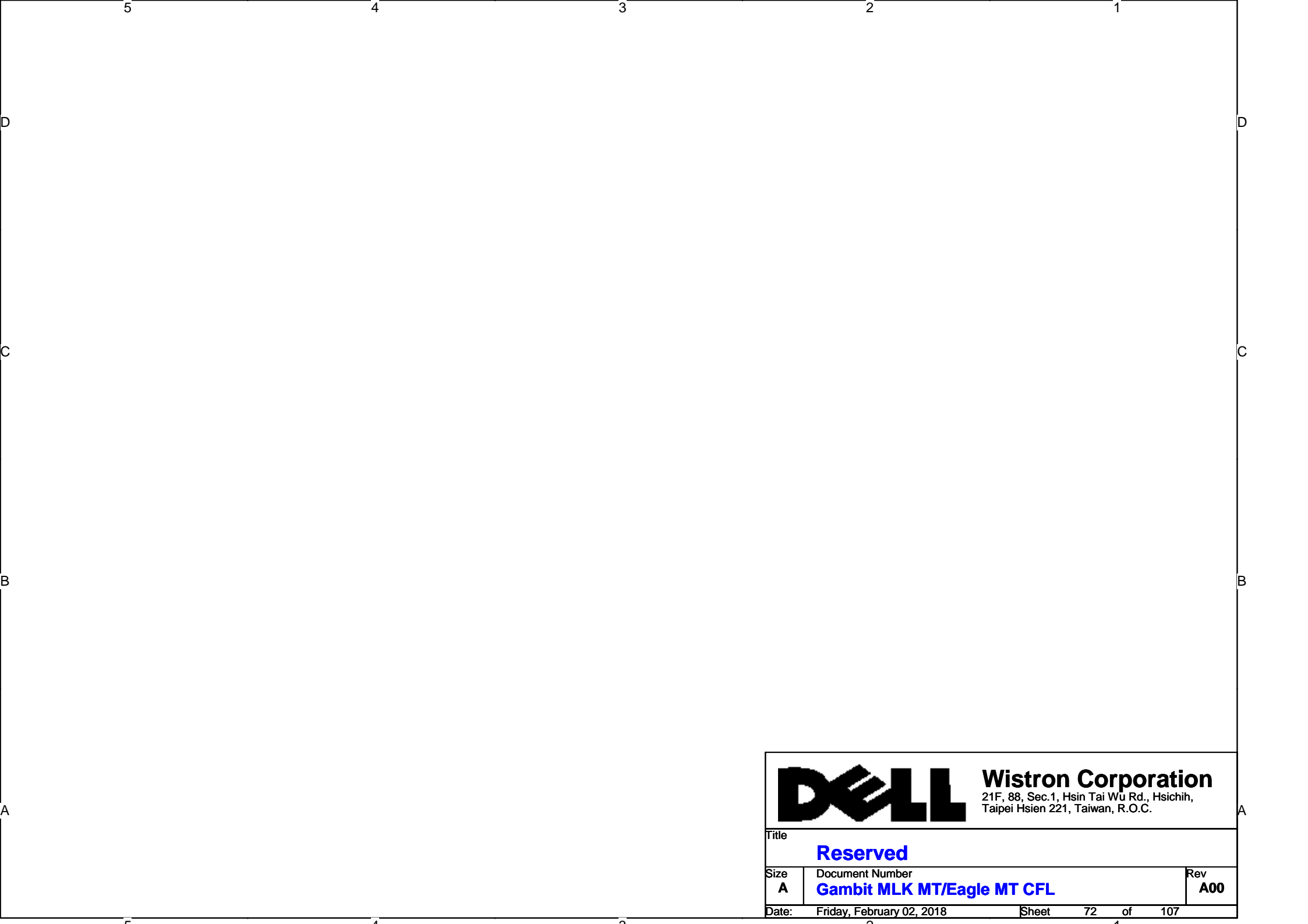



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|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | |
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| | | | | | |
| | | | | | |
| | | | | | |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| 5 | 4 | 3 | 2 | 1 | |

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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

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|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |

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| | | | | |
|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |

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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

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|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |

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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |



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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |



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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |




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| | | | | | |
|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | |
| | | | | | |
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| | | | | | |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| 5 | 4 | 3 | 2 | 1 | |

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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

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|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | |
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| | | | | | |
| | | | | | |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| 5 | 4 | 3 | 2 | 1 | |

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|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |

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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

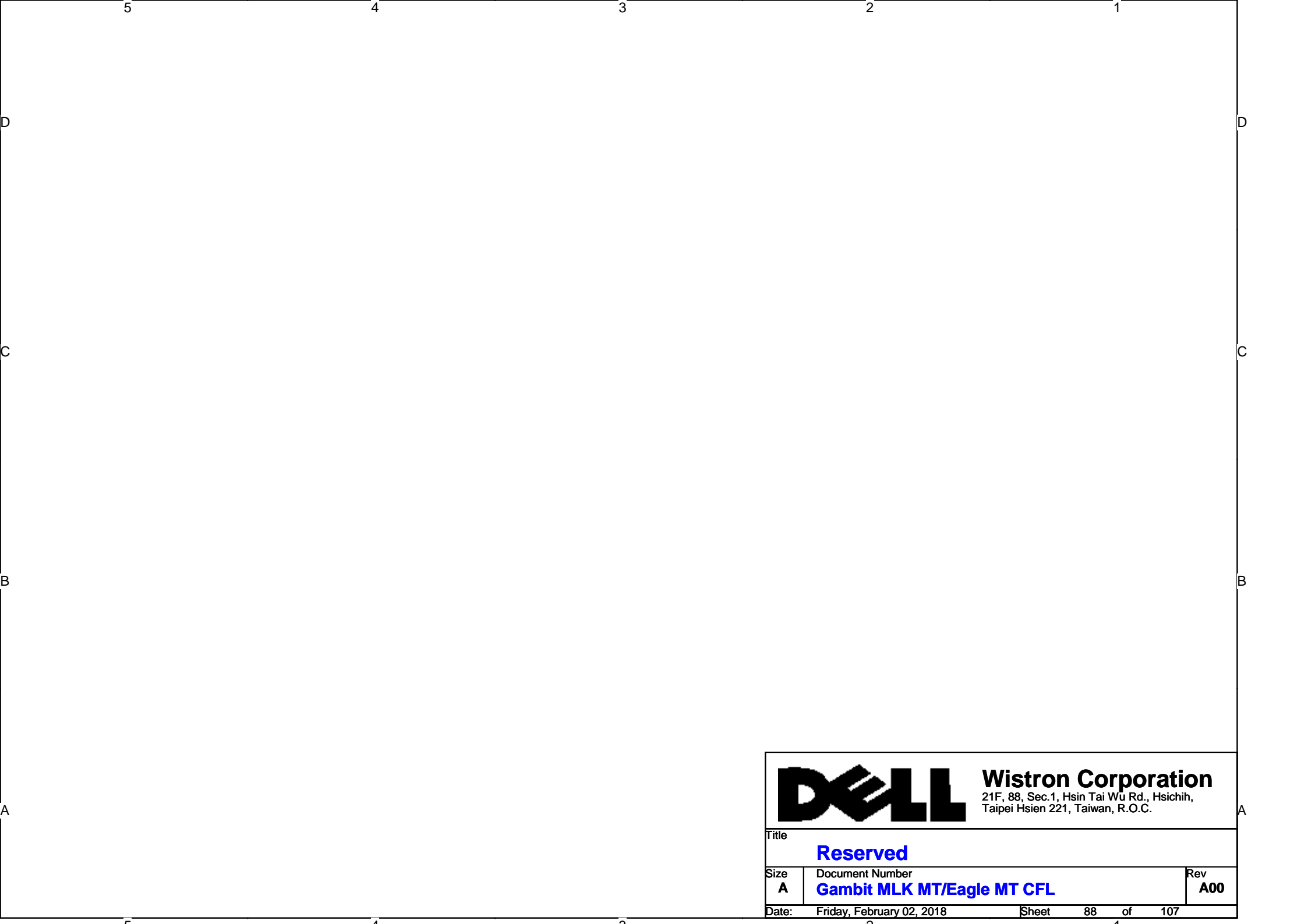



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| | | | | |
|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |

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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

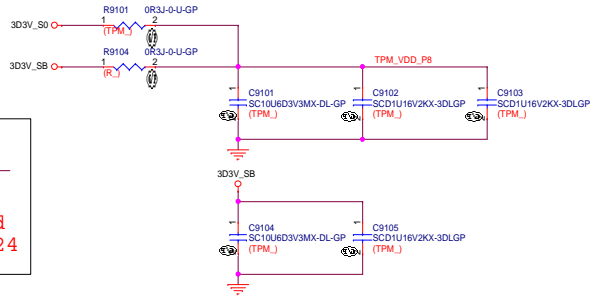


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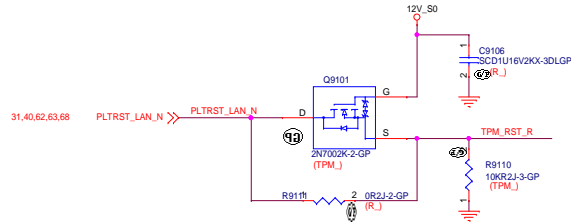
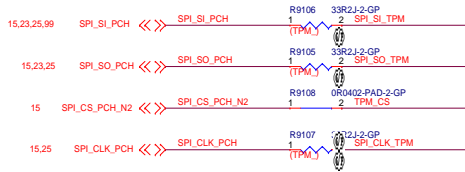
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|----------|----------------------------|-----------------|
| Title | | |
| Reserved | | |
| Size | Document Number | Rev |
| A | Gambit MLK MT/Eagle MT CFL | A00 |
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| | | | | | |
|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | |
| | | | | | |
| | | | | | |
| | | | | | |
| | | | | | |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| 5 | 4 | 3 | 2 | 1 | |

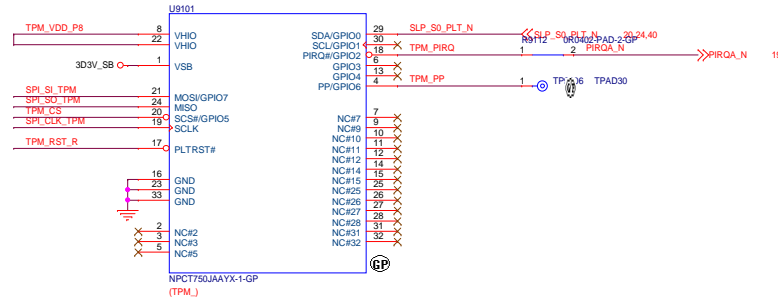
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R9113 X01 have to add
modfiy by bob 20170724

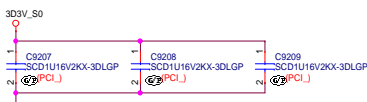
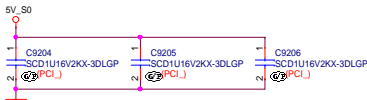


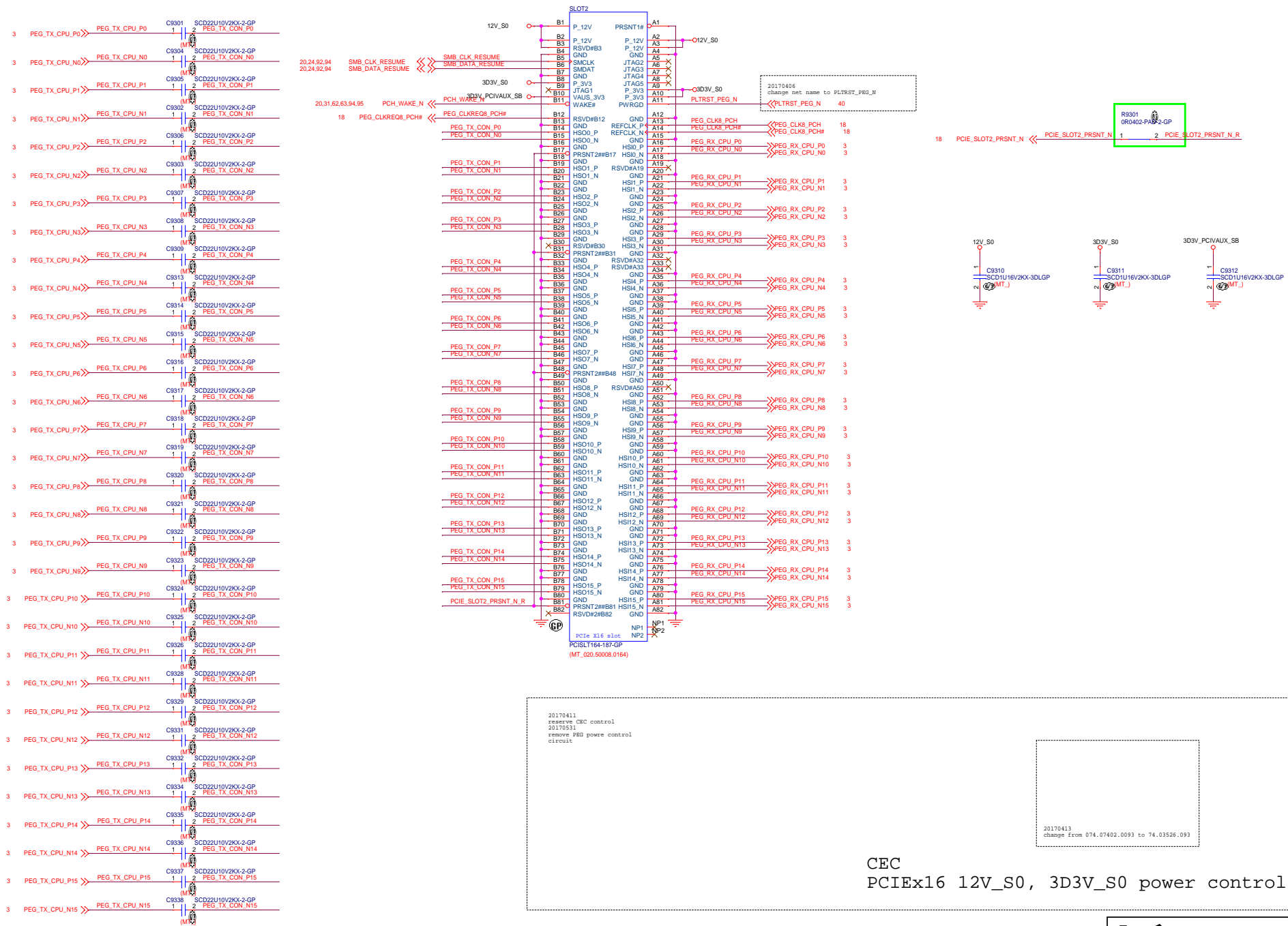
Nuvoton TPM



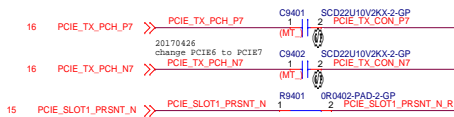
```
20170821
add PCI_D8T Pull-up 10K by Bob

20170831
Delete PCI_D8T Pull-up 10K by Bob
```





CEC
PCIEx16 12V_S0, 3D3V_S0 power control



20,24,92,93,94
20,24,92,93,94

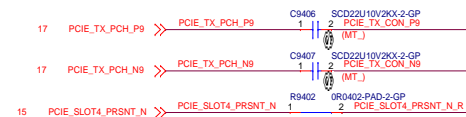
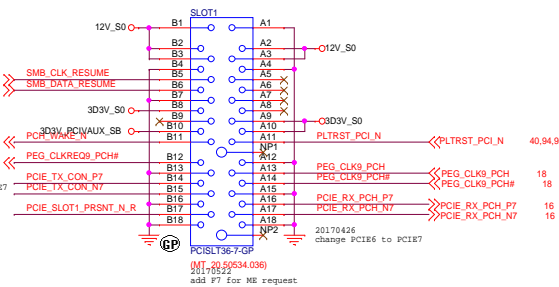
SMB_CLK_RESUME
SMB_DATA_RESUME

20,31,62,63,93,94,95

PCH_WAKE_N

18 PEG_CLKREQ0_PCH#

20170426
change PCIE6 to PCIE7



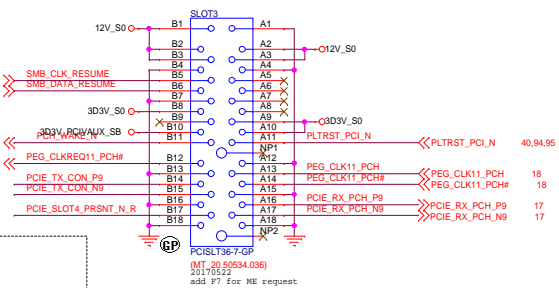
20,24,92,93,94
20,24,92,93,94

SMB_CLK_RESUME
SMB_DATA_RESUME

20,31,62,63,93,94,95

PCH_WAKE_N

18 PEG_CLKREQ11_PCH#




CEC
PCIVAUX power control



| | | |
|-------|---------------------------|----------------------------|
| File | | PCIEX1/X4 |
| Size | | Document Number |
| C | | Gambit MLK MT/Eagle MT CFL |
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| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |




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| Reserved | | |
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| | | | | |
|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 |
| D | | | | D |
| C | | | | C |
| B | | | | B |
| A | | | | A |
| 5 | 4 | 3 | 2 | 1 |

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|---|--|---|
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| Title Reserved | | |
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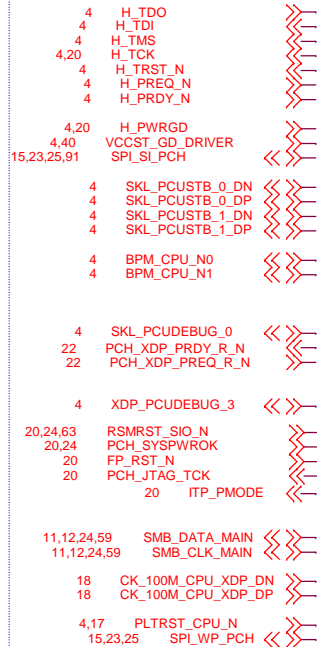
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|---|---|---|---|---|---|
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| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |



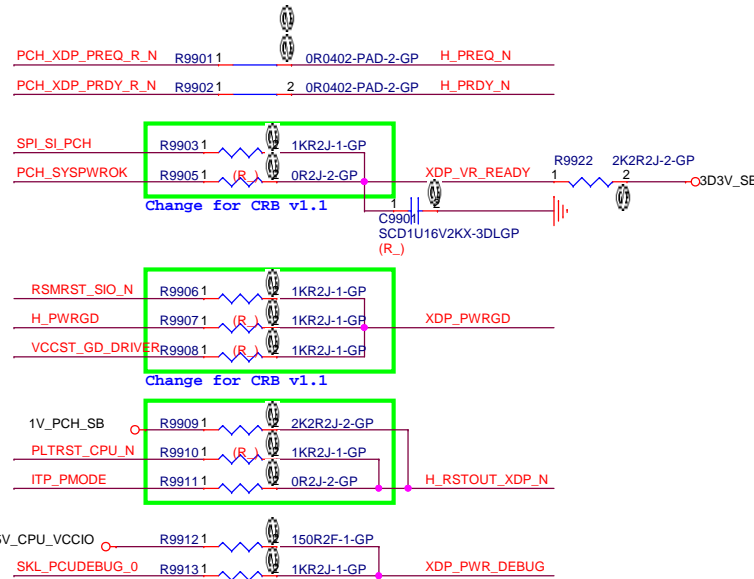
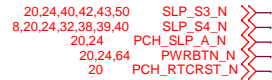
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| Title | | |
| Reserved | | |
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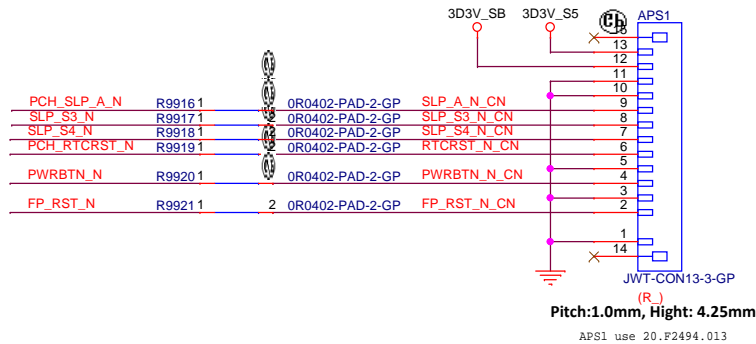
XDP for CPU



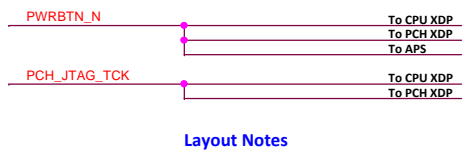
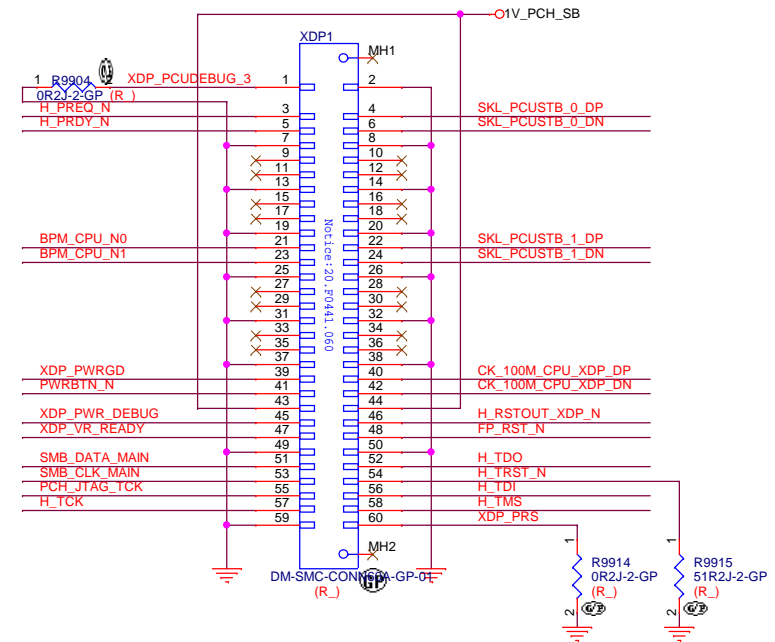
APS DEBUG



APS CONNECTOR



XDP for CPU




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Title XDP&ITP

Size B Document Number Gambit MLK MT/Eagle MT CFL Rev A00

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| | | | | | |
|---|---|---|---|---|---|
| 5 | 4 | 3 | 2 | 1 | |
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| | | | | | |
| | | | | | |
| | | | | | |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| 5 | 4 | 3 | 2 | 1 | |

| | | |
|---|--|---|
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| Title |
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Reserved

Size

A

Document Number

Gambit MLK MT/Eagle MT CFL

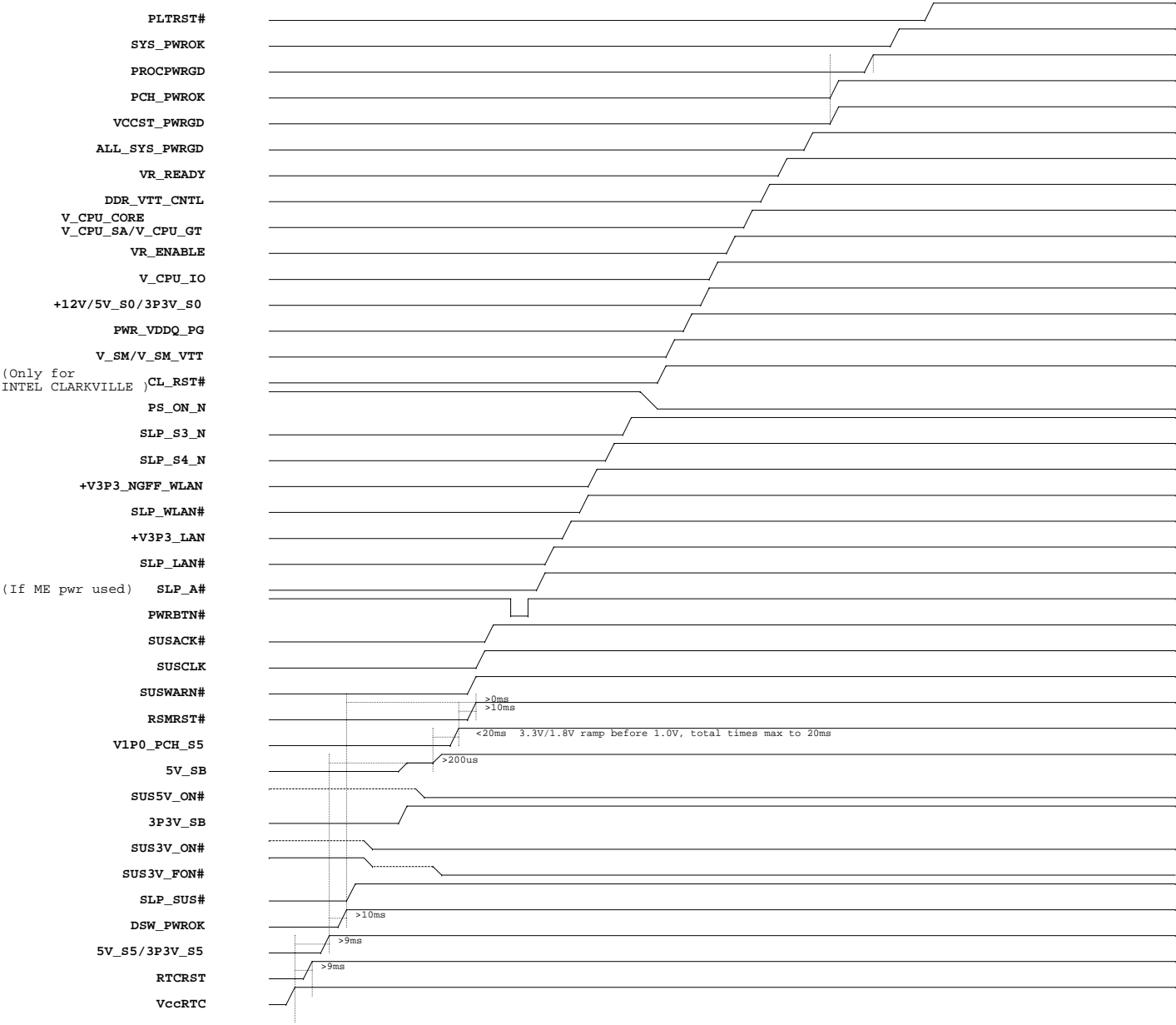
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| Rev | |
|-----|--|

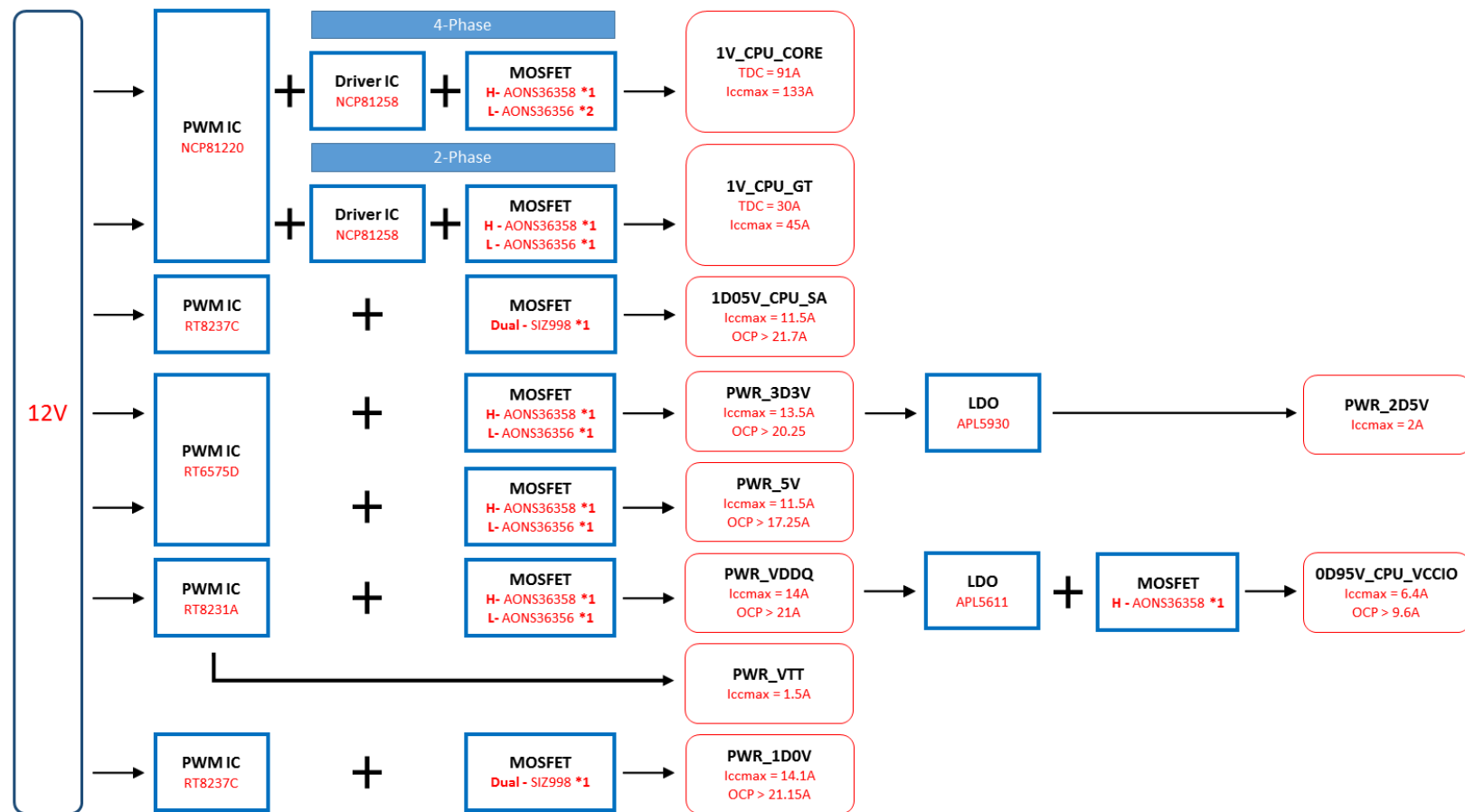
A00

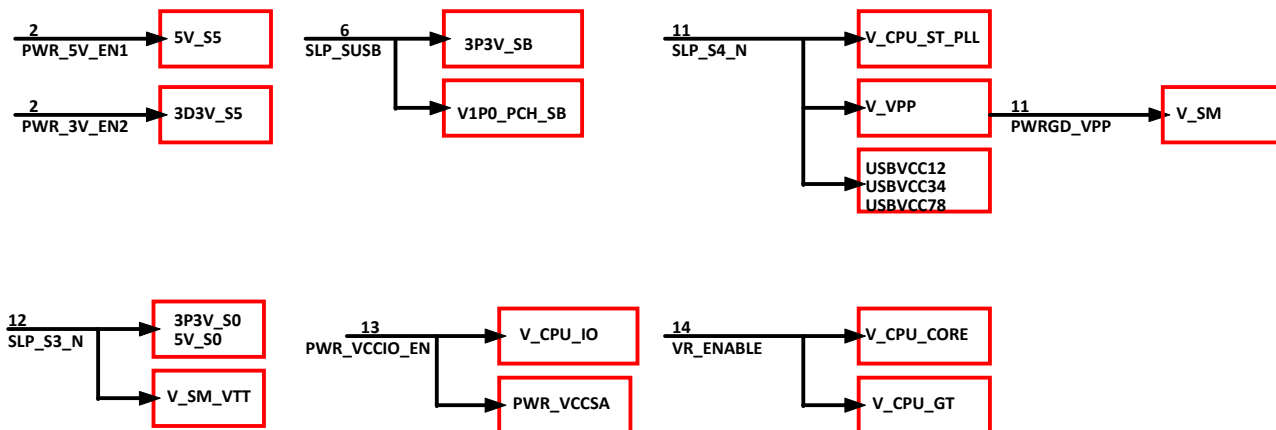
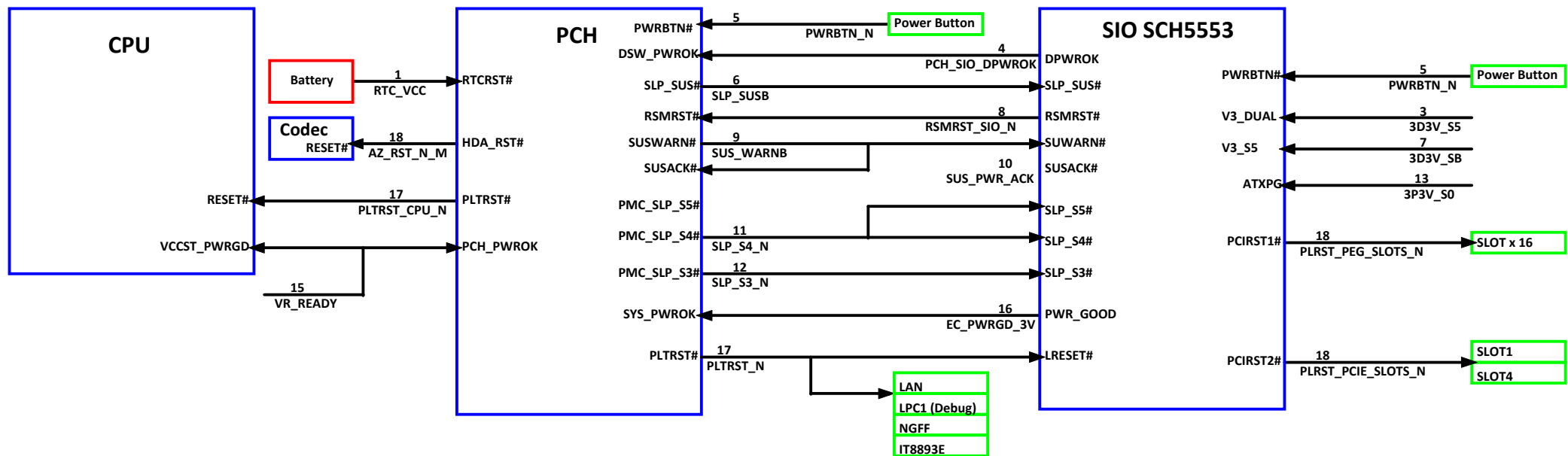
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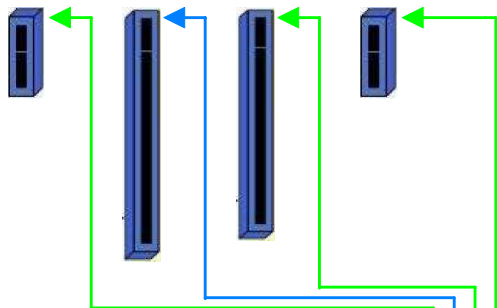
POWER ON SEQUENCE







SLOT4 SLOT3 SLOT2 SLOT1



INTEL
Kaby Lake-S
(65W 4C + GT2)

SKT H4 LGA1151
42.5 mm x 42.5 mm



Channel A

2133MHz/2400MHz

DDR4 DIMM

Unbuffered 8GB

Channel B

2133MHz/2400MHz

DDR4 DIMM

Unbuffered 8GB

INTEL PCH

Skylake

PCH-H

FCBGA 837PIN
23 mm x 23 mm



100MHz

Realtek Lan
RTL8111H

25MHz

100MHz

CPU XDP

PCH XDP

100MHz

ITE IT8893E

33MHz

100MHz

NGFF

LPC 80 Port

SIO
SMSC SCH5553

24MHz

24MHz


24MHz

32.768KHz


32.768KHz

| | Name | Type | SSC Capable | Description |
|---|--|------|-------------|--|
| | CLKOUT_ITPXPDP_P CLKOUT_ITPXPDP_N | O | Yes | Differential ITP Debug Clock: 100 MHz differential output to processor XDP/ITP connector on the platform |
| 1 | CLKOUT_CPUNSSC_P CLKOUT_CPUNSSC_N | O | No | Unfiltered Clock from Crystal to CPU: 24 MHz differential re-buffered crystal reference clock to the processor |
| 2 | CLKOUT_CPUPCIBCLK_P CLKOUT_CPUPCIBCLK_N | O | Yes | Differential PCIe* Reference Clock to CPU: 100 MHz PCIe* 3.0 specification compliant differential PCIe* reference clock to the processor |
| 3 | CLKOUT_CPUBCLK_P CLKOUT_CPUBCLK_N | O | Yes | Differential Clock to CPU: 100 MHz differential core reference clock to the processor |
| | CLKOUT_SRC_P[15:0] CLKOUT_SRC_N[15:0] | O | Yes | PCI Express* Clock Output: 100 MHz PCIe* 3.0 specification compliant differential output clocks to PCIe* devices |
| | CLKOUT_LPC[1:0] | O | No | LPC Clock Outputs: Single-Ended 24 MHz output to various single load connectors/devices |
| | CLKOUT_48 | O | No | 48 Clock Output (SKL-H Server Only): Single-Ended 48 MHz output to Server BMC devices |
| | SRCLCKRQ#[15:0] | I/O | N/A | Clock Request: Clock request signals for PCIe* 100 MHz differential clocks |
| | XTAL24_IN | I | N/A | Crystal Input: Input connection for 24 MHz crystal to PCH oscillator circuit |
| | XTAL24_OUT | O | N/A | Crystal Output: Output connection for 24 MHz crystal to PCH oscillator circuit |

| | | | | | |
|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |

| | |
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| Title <div>REST Flow Chart</div> | |
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|---|---|---|---|---|---|
| | 5 | 4 | 3 | 2 | 1 |
| D | | | | | D |
| C | | | | | C |
| B | | | | | B |
| A | | | | | A |
| | 5 | 4 | 3 | 2 | 1 |



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